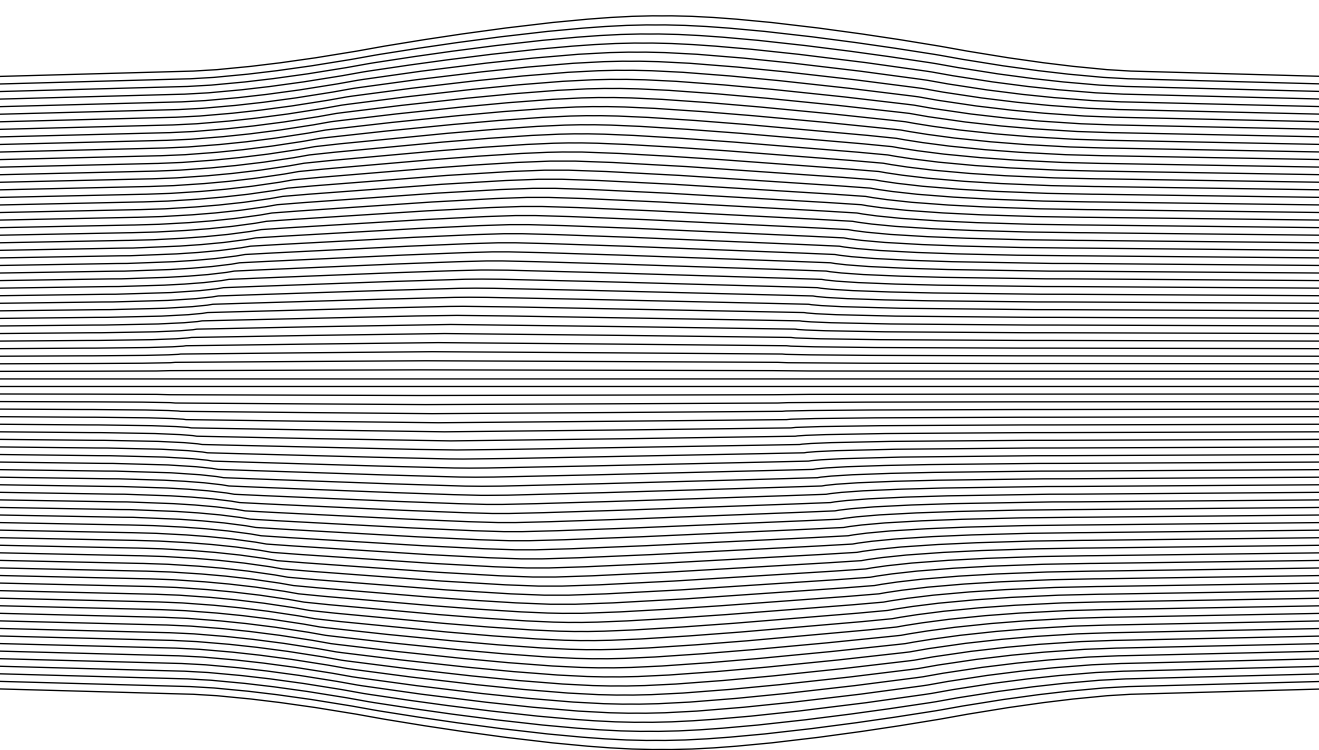


# GPC-BASIC

SUPPLEMENTARY

MITSUBISHI PROGRAMMABLE CONTROLLER

MELSEC



**MITSUBISHI**

# CONTENTS

## 1. AD51 SYSTEM SUBROUTINES

1-1 ~ 1-9

1.1 Retry Time Setting .....	1-3
1.2 Setting Data for Calling System Subroutines .....	1-4
1.3 System Subroutine Execution Results .....	1-9

## 2. BASIC COMMANDS

2-1 ~ 2-9

CLOSE .....	2-2
LOCATE .....	2-3
OPEN .....	2-4
ZIDV .....	2-7
ZODV .....	2-8

## 3. SYSTEM SUBROUTINES

3-1 ~ 3-35

3.1 System Subroutines Which Do Not Access to PC CPU .....	3-1
SCB .....	3-2
SCA .....	3-3
SHX .....	3-4
SHD .....	3-6
STC .....	3-7
SRP .....	3-8
3.2 System Subroutines Which Access to PC CPU .....	3-9
SPC .....	3-10
SKC .....	3-11
SKR .....	3-12
SKP .....	3-13
SR2 .....	3-14
SW2 .....	3-15
SADR .....	3-16
SADW .....	3-18
SADT .....	3-20
SADM0 .....	3-23
SADM1 .....	3-26
SAAR .....	3-27
SAAW .....	3-28

SAPR	3-30
SAPW	3-31
SAPS	3-32
SIT	3-33
SIR	3-34
SC2	3-35

# 1. AD51 SYSTEM SUBROUTINES

Table 1 indicates the system subroutines used to access the Programmable Controller CPU from the AD51.

Item		System Sub-routine	Processing	Number of Points Processed during One Communication	PC CPU State		
					STOP	RUN	
Device memory	Batch read	Bit	Reads data from bit devices (such as X, Y, and M) in units of 1 point.	256 points	○	○	
		Word	SADR	Reads data from bit devices (such as X, Y, and M) in units of 16 points.			32 words (512 points)
				Reads data from word devices (such as D and R) in units of 1 point.			64 points
	Batch write	Bit	Writes data to bit devices (such as X, Y, and M) in units of 1 point.	160 points	○	○	
		Word	SADW	Writes data to bit devices (such as X, Y, and M) in units of 16 points.			10 words (160 points)
				Writes data to word devices (such as D and R) in units of 1 point.			64 points
	Test (random write)	Bit	SADT	Randomly specifies bit devices (such as X, Y, and M) and device numbers in units of 1 point and sets/resets them.	20 points	○	○
		Word		Randomly specifies bit devices (such as X, Y, and M) and device numbers in units of 16 points and sets/resets them.	10 words (160 points)		
				Randomly specifies word devices (such as D and R) and device numbers in unit of 1 points and writes data to them.	10 points		
	Monitor data entry	Bit	SADMO	Sets bit devices to be monitored (such as X, Y, and M) in units of 1 point.	40 points*	○	○
		Word		Sets bit devices to be monitored (such as X, Y, and M) in units of 16 points.	20 words* (320 points)		
				Sets word devices to be monitored (such as D and R) in units of 1 point.	20 points		
Monitor	Bit	SADM1	Monitors devices for which monitor data entry has been executed.	/	○	○	
	Word						
Sequence program	Read	Main	Reads main sequence program.	64 steps	○	○	
		Sub	Reads subsequence program.				
	Write	Main	Writes main sequence program.				
		Sub	Writes subsequence program.				○

Table 1 System Subroutine List

Item		System Sub-routine	Processing	Number of Points Processed during One Communication	PC CPU State	
					STOP	RUN
Parameter	Read	SAPR	Reads parameters from PC CPU.	128 bytes	○	○
	Write	SAPW	Writes parameters to PC CPU.		○	×
	Analysis request	SAPS	Causes PC CPU to recognize and check rewritten parameters.		○	×
PC CPU	Remote RUN	SKR	Requests remote RUN of PC CPU.			
	Remote STOP	SKP	Requests remote STOP of PC CPU.			
	PC type mode	SPC	Reads PC CPU type (A0J2, A1, A2, or A3).		○	○
Buffer memory	Batch read	SR2	Read data from buffer memory.	128 bytes	○	○
	Batch write	SW2	Writes data to buffer memory.		○	○

**Table 1 System Subroutine List (continued)**

In the PC CPU State column of the above table, ○ indicates that the system subroutine can be executed and × indicates that it cannot be executed.

For the number of points marked \*, the value is half when the device is X (input).

## 1.1 Retry Time Setting

The AD51 buffer memory can only be accessed from one side at a time, therefore if the AD51 attempts access while the PC CPU is accessing the buffer memory, the AD51 must wait for a period of time specified as the "retry time" before re-trying for access.

At power-on or AD51 reset time, retry time is 10msec. Using system "SC2," it can be changed into 0 to 255msec. A retry time value is common to all tasks. If retry time is set to 0, retry is not executed.

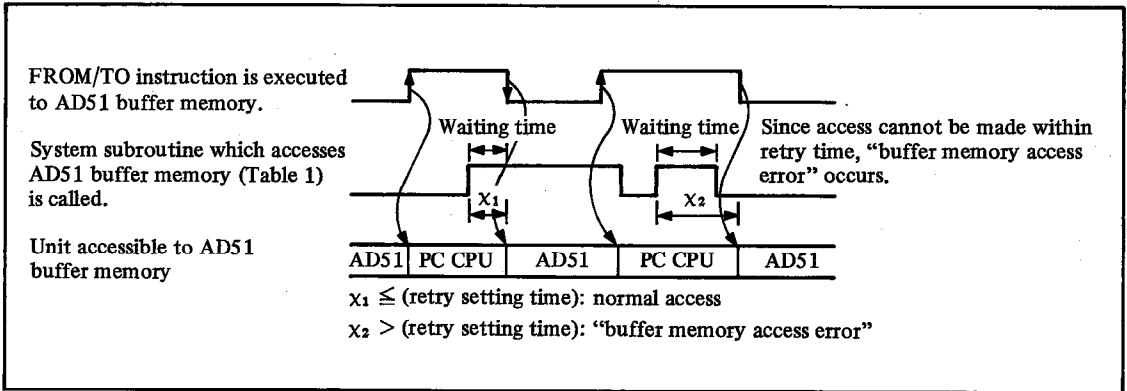


Fig. 1 Retry Time

## 1.2 Setting Data for Calling System Subroutines

### (1) PC No.

PC No. must be set as FFH.

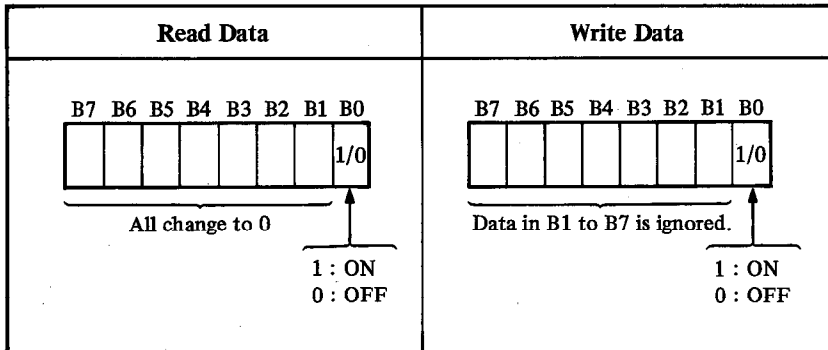
### (2) Bit/word specification

Specify bit or word in which data will be handled.

Bit/Word Specification	Character Setting
Bit specification	B (42H)
Word specification	W (57H)

[Bit specification]

Bit devices are accessed in units of 1 point. Word devices cannot be accessed.  
Handled data configuration is as shown below.



[Word specification]

Both word devices and bit devices can be specified. To read and write data from and to word devices, always specify "word."

Bit devices are accessed in units of 1 word (16 points). ON/OFF data of 16 points from (head device) to (head device + 15) is stored in order, beginning with B0. If data is ON, 1 is stored. If it is OFF, 0 is stored. If the head device number is X10, data configuration is as shown below.

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
X1F	X1E	X1D	X1C	X1B	X1A	X19	X18	X17	X16	X15	X14	X13	X12	X11	X10

(3) Head device

To set the head device to be accessed to, be careful of the following points. Table 2 shows device setting ranges.

1) Bit devices and word devices are classified as follows:

Bit devices – X, Y, M, L, B, F, T (contact), T (coil), C (contact), C (coil)

Word devices – T (present value), C (present value), D, W, R

2) For word specification, always set a bit device number to a multiple of 16.

3) Specify a device number with five characters (ASCII) in the range shown in Table 2. "0" in upper digits (e.g.  $\sim$  area of X0070) may be specified using a blank code (20H).

4) Although M and L ranges are specified, the same processing will be executed if L is specified in the M number range or vice versa.



Bit Device			Word Device		
Device	Device number range (Character)	Deci/Hexa	Device	Device number range (Character)	Deci/Hexa
Input X	X0000 to X07FF	Hexa	Timer (present value) T	TN000 to TN255	Deci
Output Y	Y0000 to Y07FF	Hexa		Counter (present value) C	CN000 to CN255
Internal relay M	M0000 to M2047	Deci	Data register D		D0000 to D1023
Latch relay L	L0000 to L2047	Deci	Link register W	W0000 to W03FF	Hexa
Link relay B	B0000 to B03FF	Hexa	File register R	R0000 to R8191	Deci
Annunciator F	F0000 to F0255	Deci		Special register D	D9000 to D9255
Special relay M	M9000 to M9255				
Timer (contact) T	TS000 to TS255				
Timer (coil) T	TC000 to TC255				
Counter (contact) C	CS000 to CS255				
Counter (coil) C	CC000 to CC255				

**Table 2 Device Setting Ranges**

In the above table, Deci indicates decimal and Hexa hexadecimal.

**(4) Main/sub specification**

To read and write a sequence program and T/C set value, specify main program or subprogram. For read and write from and to the A1, A2, or A0J2CPU, always specify main program.

Program	Character Setting
Main program	M (4DH)
Subprogram	S (53H)

(5) Head steps for read and write

For read and write of T/C set values, specify the following numbers.

Sequence Program	Step
T0 set value	FE00H
T1 set value	FE01H
⋮	⋮
T255 set value	FEFFH
C0 set value	FF00H
C1 set value	FF01H
⋮	⋮
C255 set value	FFFFH
Step 0	0000H
Step 1	0001H
⋮	⋮
Step 30719 (30K)	77FFH

Specified step calculation

Timer:  $T_m = FE00H + n$

Counter:  $C_m = FF00H + n$

where m = device number

n = hexadecimal value converted from device number

(6) T/C set values

For read and write of T/C set values, specify the following numbers.

Constant Specification	Set Value	Data Register Specification	Set Value
K0	0000H	D0	8000H
K1	0001H	D1	8002H
K2	0002H	D2	8004H
⋮	⋮	⋮	⋮
K32766	7FFE H	D1022	81FCH
K32767	7FFFH	D1023	81FEH

(7) Time check value

When the AD51 accesses the PC CPU, set wait time (from when the AD51 provides a processing request to the PC CPU to when the PC CPU gives a reply) in units of 10msec. If an access to the PC CPU is not complete within the time check period, a "time out error" occurs. Set values are 2 to FFFFH (20 to 655350msec). 0 or 1 is regarded as 2 (20msec).

An access from the AD51 to the PC CPU is made when the END, FEND, or COM instruction is executed in the sequence program. If processing requests equivalent to the access from the AD51 to the PC CPU (five types given below) are executed simultaneously, these request processings are executed one by one. Therefore, 1 to 5 scans may be required until they are executed.

1. PC CPU's OS program processing request
2. Processing request from a peripheral (A6GPP, etc.)
3. Processing request from an optical or coaxial data link unit loaded in the CPU unit  
A1CPUP21/R21, A2CPUP21/R21, A3CPUP21/R21
4. Processing request from an optical or coaxial data link unit for three-tier master station  
AJ71P22, AJ72R22
5. Processing request from AJ71C24 or second AD51

[Example]

If the PC CPU scan time is 100msec and processing requests are given from the A6GPP and AJ71C24, each access from the AD51 to the PC CPU is processed 1 to 3 scans. Hence, set 30 (300msec) or a larger time check value.

### 1.3 System Subroutine Execution Results

As an execution result of a system subroutine in Table 1 which accesses from the AD51 to the PC CPU, an error code is written to registers (H) and (L). Listed below are common codes. For other codes, refer to respective system subroutines.

Code	Error	Remarks
2	PC access error	PC CPU hardware fault.
4	Input data error	Setting data for system subroutine execution is wrong.
5	Write (or entry) data error	Data set to an address specified at (B)(C)+4, +5 is wrong.
6	No data entered	Device has not been entered using system subroutine SADM0.
7	PC RUN	Access cannot be made during PC CPU RUN.
8	Buffer memory access error	Increase retry time using system subroutine "SC2."
9	Time out error	Processing has not been completed within a time check period.
10	PC down error	PC CPU has been reset or is down.
-1	PC No. error	The set PC No. is not accessible.
-4	Other data error	<ul style="list-style-type: none"> <li>• Subprogram has been specified for the A0J2, A1 or A2CPU, or the A3CPU which has no subprogram.</li> <li>• Write has been attempted to ROM area of the PC CPU.</li> </ul>
-9	Remote error	Remote RUN/STOP is being executed from another unit.
-17	Link error	Fault has occurred in MELSEC-NET.

## 2. BASIC COMMANDS

BASIC commands described in this chapter have been added or corrected to the AD51. For details, refer to relevant pages.

Command	Reference Page
CLOSE	2-2
LOCATE	2-3
OPEN	2-4
ZIDV	2-7
ZODV	2-8

# CLOSE

TYPE | D

PRG

## FUNCTION

Closes the channel of RS-232C or RS-422.

## FORM

CLOSE channel number

## EXPLANATION

- Closes the channel of RS-232C or RS-422 opened by the OPEN command.
- Specify [channel number] which is the same as the channel number specified by the OPEN command.

**CAUTION**

Data, which remain in the send/receive buffer after the CLOSE command is executed, are disabled.

## EXAMPLE

```
OK
>LIST
100 REM "EXERCISE"
110 OPEN $4, $5C, $37, 4 .....Channel 4 of RS-232C is opened and placed in send/
120 FOR I=0 TO 10 .....receive enable state.
130 A=I*I
140 ZODV2
150 PRINT A
160 NEXT I
170 ZTIME 300
180 CLOSE $4 .....Channel 4 of RS-232C is closed.
190 END
OK
>
```

# LOCATE

TYPE C

PRG

## FUNCTION

Specifies the cursor position on the screen.

## FORM

LOCATE line position, column position

## EXPLANATION

- The line position and column position can also be specified by expressions.
- Ranges of the line position and column position are as shown in the table below:

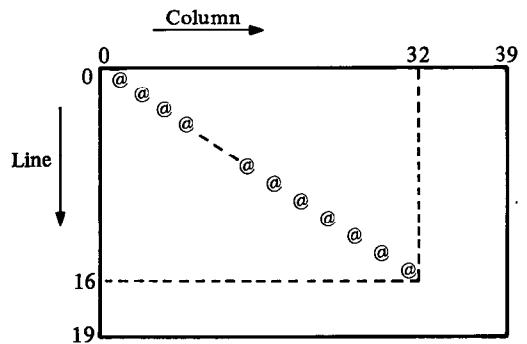
	Screen Mode
Line	0 to 128
Column	0 to 128

## EXAMPLE

The standard 640 x 400 mode screen has been specified.

```
OK
>LIST
100 REM "EXERCISE"
110 CLS
120 FOR I=0 TO 16
130 LOCATE I, I*2
140 PRINT "@"
150 NEXT I
160 END
OK
>RUN
```

As shown at right, @ is displayed from 0, 0 to 16, 32.



## NOTE

The line position and column position setting ranges can be processed by OS. The setting ranges differ depending on connected general-purpose terminals. Specify the ranges according to the specifications of a used general-purpose terminal.

# OPEN

TYPE D

PRG

**FUNCTION**

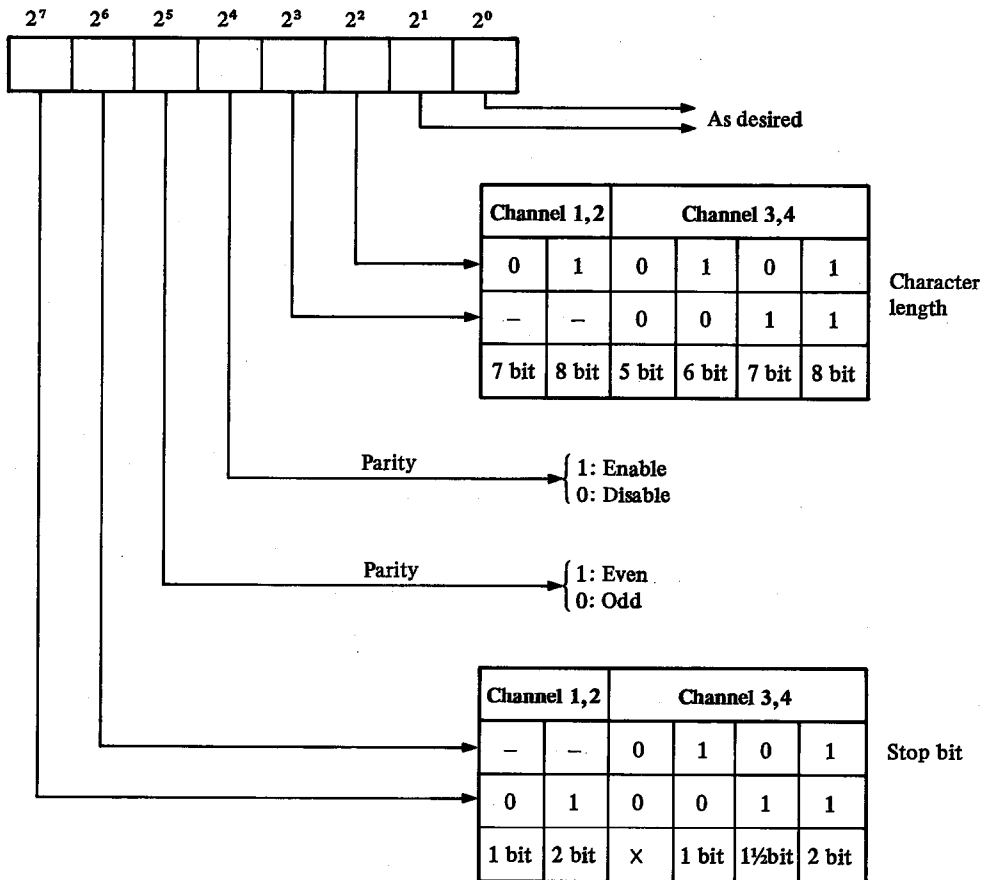
Opens the RS-232C or RS-422 channel and enables sending/receiving operations.

**FORM**

OPEN channel number, variable 1, variable 2, variable 3

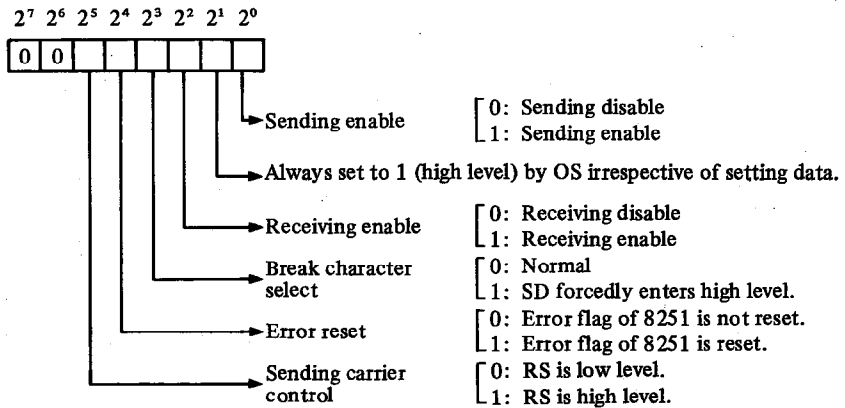
**EXPLANATION**

- Opens the RS-232C or RS-422 channel specified in [channel number].
- When the block data receiving (SRB) and block data sending (SWB) of system subroutine are used, it is required to open the channel by executing the OPEN statement.
- [channel number] is one of channels 1 to 4.
- Variable 1 is for the setting of communication mode and configured as shown in the figure below when converted into binary.





- Variable 2 is for the setting of command, each digit has the following meaning when converted into binary.



- Variable 3 is for the setting of baud rate and as shown below.

	1	2	3	4	5	6
Baud rate	300	600	1200	2400	4800	9600

#### NOTE

- For details of communication mode and command, see the instruction manual provided for LSI8251.
- The most commonly used data for variable 2 (command data) is as follows:
  - 36H – only when receiving is performed
  - 33H – only when sending is performed
  - 37H – both sending and receiving are performed
- The data terminal ready (DTR) signal for channels 1, 3, and 4 is always turned on by OS.  
The DTR signal is not available to channel 2.
- Brake character selection and sending carrier control are not available to channels 1 and 2. Therefore, set optional data.
- Data, which remains in the sending/receiving buffer upon execution of OPEN command, is disabled.

### EXAMPLE 1

```
OK
>LIST
100 REM "EXERCISE"
110 OPEN 2, $5C, $37, 4.....Predetermined setting is sent to RS-232C in channel 4
120 A=$E300                      to enable sending.
130 A(0)=$6000
140 A(1)=$4100.....2 channel data length is 256 bytes.
150 A(2)=10
160 B=CALL($0, $800C, 2, $E300).....System subroutine SWB is called.
170 END

OK
>RUN
OK
```

Data beginning with the address of \$6000 of channel 0 are sent to the equipment, which is connected to the channel 4 of RS-232C, by use of the block data sending (SWB) command. After opening the channel, make communication by the SWB and SRB commands.

### EXAMPLE 2

When it is desired to open the K6PRE or K7PRE in BASIC, set as indicated below.

```
OPEN X, $7F, $37, 4.....K6PR, K6PR-K
OPEN X, $CF, $37, 4.....K7PR
OPEN X, $7F, $37, 6.....A7PR
OPEN X, $4F, $37, 5.....KD51PR
```

(X changes depending on a connected channel.)

**FUNCTION**

Changes over the input console.

**FORM**

ZIDV channel number

**EXPLANATION**

- The ZIDV command allows the entry of data through a desired keyboard when data are entered through the keyboard by use of the INPUT command or INKEY command.
- The console used at the start of BASIC has been set to the keyboard which is connected to the channel specified using the DIP switch SW16.
- The channel numbers are as shown in the following table:

Number	Input Console and Connection Channel
0	Depends on the DIP switch SW16 on AD51 front panel. ON: RS-422 Channel 1 OFF: RS-232C Channel 3
1	RS-422 Channel 1
2	RS-422 Channel 2
3	RS-232C Channel 3
4	RS-232C Channel 4

**EXAMPLE**

```

OK
>LIST
100 REM "EXERCISE"
105 OPEN 2, $5E, $37, 4 .....Channel 2 of RS-422 is opened.
110 ZIDV 2 .....Designation of data entry in line number 120 is specified
120 A=INKEY .....for keyboard connected to RS-232C channel 2.
130 PRINT SA
140 GOTO 120
150 END

OK
>RUN
4 1 ..... "A" of keyboard has been pressed.
4 2 ..... "B" of keyboard has been pressed.
4 3 ..... "C" has been pressed.
4 4 ..... "D" of keyboard has been pressed.

```

**FUNCTION**

Changes over the output console.

**FORM**

ZODV channel number

**EXPLANATION**

- The ZODV command allows the output of data to a desired output console when data are output by the following command:

Command Name	Command Name
CLS	ZCOFF
ZNOR	ZCON
LOCATE	ZCRV
PRINT	

- At the start of BASIC, the output console has been set to the CRT which is connected to the channel specified using the DIP switch SW16.

Number	Output Console and Connection Channel
0	Depends on the DIP switch SW16 on AD51 front panel. ON: RS-422 Channel 1 OFF: RS-232C Channel 3
1	RS422 Channel 1
2	RS-422 Channel 2
3	RS-232C Channel 3
4	RS-232C Channel 4

```
OK
>LIST
 100 REM "EXERCISE"
 105 OPEN 1, $50, $37, 5.....Channel 1 of RS-232C is opened.
 110 ZODV 1.....Output console connected to channel 1 of RS-232C is
 120 PRINT "MITSUBISHI"      specified.
 130 END

OK
>RUN....."MITSUBISHI" is displayed on output console connected
OK      to channel 1 of RS-232C.
>
```

### 3. SYSTEM SUBROUTINES

System subroutines added to the AD51 can be largely classified into those which access to the PC CPU and those which do not access.

#### 3.1 System Subroutines Which Do Not Access to PC CPU

System Subroutine	Reference Page
SCB	3-2
SCA	3-3
SHX	3-4
SHD	3-6
STC	3-7
SRP	3-8

# SCB

TYPE	B
------	---

## FUNCTION

Reads the present time from the clock element and stores it in the memory address specified in the (B) and (C) registers and the following addresses.

## INPUT

(D), (E) registers . . . . . Channel which stores the time read from the clock element.

(B), (C) registers . . . . . Head address of memory which stores the time read from the clock element.

## OUTPUT

The execution result of SCB is stored in (H) and (L) registers.

(H), (L) registers	Judgement
0	Storage of time read from clock element in the address specified in (B)(C) registers and following addresses has been completed normally.
1	Channel error [(D), (E) register value cannot be used for the channel.]
2	Time out (Clock element is not placed in read state even after a predetermined time has elapsed.)

(B)(C) + 0	Second
1	Minute
2	Hour
3	Day
4	Month
5	Year

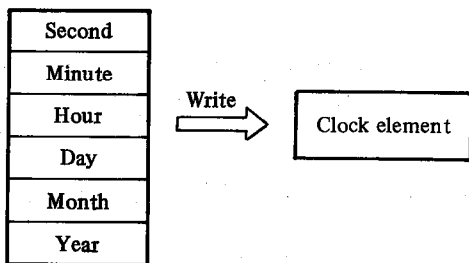
<b>NOTE</b>
All the data of read time are stored in binary notation.

# SCA

**TYPE B**

**FUNCTION**

Writes the set data of year, month, day, hour and minute to the clock element.



**INPUT**

(D), (E) registers . . . . . Set the channel which stores the set data.

(B), (C) registers . . . . . Set the head address of set data.

Set data . . . . . Set year, month, day, hour and minute to (B)(C) + 0 to 5.

(B)(C) +0	Second
1	Minute
2	Hour
3	Day
4	Month
5	Year

**OUTPUT**

The execution result of SCA is stored in (H) and (L) registers.

(H), (L) registers	Judgement
0	Write to clock element has been completed normally.
1	Channel error [(D), (E) register value cannot be used for the channel.]
4	Data error (Set data has error.)

**NOTE**  
Specify all the set data in binary notation.



# SHX

TYPE	B
------	---

## FUNCTION

Controls the data sending and receiving of RS-232C or RS-422 channel.

### During sending

- When the Xoff code is received, stops data sending to exterior.
- When the Xon code is received, resumes data sending to exterior.

### During receiving

- When the number of bytes in the vacant area of receive buffer is 7 or less, sends the Xoff code.
- When the number of bytes in the vacant area of receive buffer is 32 or more, sends the Xon code.

Xon Code	Xoff Code
11H	13H

## INPUT

(D), (E) registers      Set the channel of RS-232C or RS-422.

## OUTPUT

The execution result of SHX is stored in the (H) and (L) registers.

(H), (L) Registers	Judgement
0	Execution of SHX has been completed normally.
1	Channel error

## NOTE

1. Data sending can be controlled by the Xon/Xoff codes on the external computer or personal computer side.
2. After this subroutine is called, Xon and Xoff codes are placed in 11H and 13H, respectively.

3. XON/XOFF control is not enabled for the A6GPP.

If this subroutine is called using the A6GPP as a console, the A6GPP regards the XON/XOFF code simply as data.

4. By calling SHD, control using the DTR terminal is restored.

5. Since sending control is not enabled for CH2, selection of CH2 results in an error.

# SHD

TYPE	B
------	---

## FUNCTION

After called, this subroutine controls the data sending of used channel by the DSR (Data Set Ready) terminal.

During sending	DSR State	High Level	Low Level
	Execution/non-execution of sending	Execution	Non-execution

## INPUT

(D), (E) registers . . . Set the used channel. (1 to 4)

## OUTPUT

The execution result of SHD is stored in the (H) and (L) registers.

(H), (L) Registers	Judgement
0	Execution of SHD has been completed normally.
1	Channel error

<b>NOTE</b>
<ol style="list-style-type: none"><li>1. During receiving, if 7 or less bytes have become vacant in the receive buffer of the AD51, DTR is turned off. If 32 or more bytes have become vacant in the receive buffer of the AD51, DTR is turned on.</li><li>2. During sending, if 5 or more bytes are vacant in the receive buffer of the receiving end, turn off DTR.</li><li>3. The Xon and Xoff codes are treated as data.</li><li>4. At power-on, SHD is regarded as having been selected. For channel 2 of RS422, there are no DSR and DTR terminals and sending/receiving control is not executed.</li></ol>



# SRP

## FUNCTION

Reads RS232C and RS422 port status.

## INPUT

(D), (E) registers . . . . . Port channel (1 to 4)

## OUTPUT

The execution result of SRP is stored into (H) and (L) registers.

(H), (L) Registers	Judgement
Other than -1	Normal completion of SRP
-1	Channel error

Upon normal completion, 0 is stored into the (H) register and the following data into the (L) register.

Channel Number	(L) Register Contents																
Channel 1	<table border="1"> <thead> <tr> <th>B7</th> <th>B6</th> <th>B5</th> <th>B4</th> <th>B3</th> <th>B2</th> <th>B1</th> <th>B0</th> </tr> </thead> <tbody> <tr> <td>RDRF</td> <td>OVRN</td> <td>PE</td> <td>FE</td> <td>RIF</td> <td><math>\overline{\text{DCD}}_0</math></td> <td>TDRE</td> <td>TIE</td> </tr> </tbody> </table>	B7	B6	B5	B4	B3	B2	B1	B0	RDRF	OVRN	PE	FE	RIF	$\overline{\text{DCD}}_0$	TDRE	TIE
B7	B6	B5	B4	B3	B2	B1	B0										
RDRF	OVRN	PE	FE	RIF	$\overline{\text{DCD}}_0$	TDRE	TIE										
Channel 2	<table border="1"> <thead> <tr> <th>B7</th> <th>B6</th> <th>B5</th> <th>B4</th> <th>B3</th> <th>B2</th> <th>B1</th> <th>B0</th> </tr> </thead> <tbody> <tr> <td>RDRF</td> <td>OVRN</td> <td>PE</td> <td>FE</td> <td>RIE</td> <td>CTS1E</td> <td>TDRE</td> <td>TIE</td> </tr> </tbody> </table>	B7	B6	B5	B4	B3	B2	B1	B0	RDRF	OVRN	PE	FE	RIE	CTS1E	TDRE	TIE
B7	B6	B5	B4	B3	B2	B1	B0										
RDRF	OVRN	PE	FE	RIE	CTS1E	TDRE	TIE										
Channel 3	<table border="1"> <thead> <tr> <th>B7</th> <th>B6</th> <th>B5</th> <th>B4</th> <th>B3</th> <th>B2</th> <th>B1</th> <th>B0</th> </tr> </thead> <tbody> <tr> <td>DSR</td> <td>SYN DET</td> <td>FE</td> <td>OE</td> <td>PE</td> <td>TxE</td> <td>RxRDY</td> <td>TxRDY</td> </tr> </tbody> </table>	B7	B6	B5	B4	B3	B2	B1	B0	DSR	SYN DET	FE	OE	PE	TxE	RxRDY	TxRDY
B7	B6	B5	B4	B3	B2	B1	B0										
DSR	SYN DET	FE	OE	PE	TxE	RxRDY	TxRDY										

For details of status, refer to relevant data books.

Channel 1, 2 . . . . . HD64180  
 Channel 3, 4 . . . . . M518251

### 3.2 System Subroutines Which Access to PC CPU

For input and output data for using the following system subroutines, refer to Chapter 1.

System Subroutine	Reference Page	System Subroutine	Reference Page
SPC	3-10	SADM1	3-26
SKC	3-11	SAAR	3-27
SKR	3-12	SAAW	3-28
SKP	3-13	SAPR	3-30
SR2	3-14	SAPW	3-31
SW2	3-15	SAPS	3-32
SADR	3-16	SIT	3-33
SADW	3-18	SIR	3-34
SADT	3-20	SC2	3-35
SADMO	3-23		

# SPC

TYPE	B
------	---

## FUNCTION

Judges a loaded PC CPU.

## INPUT

(D), (E) registers . . . . . FFH.  
(B), (C) registers . . . . . Time check value (10msec increments)  
20 to 655350msec

## OUTPUT

The execution result of SPC is stored into the (H) and (L) registers.

(H), (L) Registers	Contents
100	A0J2CPU
101	A1(E)CPU
102	A2(E)CPU
103	A3(E)CPU
104	A3HCPU
2	PC access error
8	Buffer memory access error
9	Time out error
10	PC down error
FFFFH(-1)	PC No. error
FFEFH(-17)	Link error

# SKC

TYPE	B
------	---

## FUNCTION

Checks the RUN/STOP state of a loaded PC CPU.

## INPUT

- (D), (E) registers . . . . . FFH
- (B), (C) registers . . . . . Time check value (10msec increments)  
20 to 655350msec (2 to FFFFH)

## OUTPUT

The execution result of SKC is stored into the (H) and (L) registers.

(H), (L) Registers	Contents
0	STOP
1	RUN
2	PC access error
8	Buffer memory access error
9	Time out error
10	PC down error
FFFFH(-1)	PC No. error
FFEFH(-17)	Link error



# SKR

TYPE	B
------	---

**FUNCTION**

Executes remote RUN of the PC CPU.

**INPUT**

(D), (E) registers ..... FFH  
 (B), (C) registers ..... Time check value (10msec increments)  
 20 to 655350msec (2 to FFFFH)

**OUTPUT**

The execution result of SKR is stored into the (H) and (L) registers.

(H), (L) Registers	Contents
0	Normal completion
2	PC access error
8	Buffer memory access error
9	Time out error
10	PC down error
FFFFH(-1)	PC No. error
FFF7H(-9)	Remote error
FFEFH(-17)	Link error

NOTE		
For remote RUN, whether RUN is executed after the data memory is cleared or not is determined depending on the status of special relays M9016 and M9017.		
Special Relay		Data Memory State
M9016	M9017	
OFF	OFF	RUN is executed without clearing the data memory.
OFF	ON	The data memory, other than the latch ranges set in the parameters, is cleared. (Link X images are not cleared.)
ON	ON/OFF	RUN is executed after all the data memory is cleared.

# SKP

TYPE	B
------	---

## FUNCTION

Executes remote STOP of the PC CPU.

## INPUT

(D), (E) registers . . . . . FFH

(B), (C) registers . . . . . Time check value (10msec increments)  
20 to 655350msec (2 to FFFFH)

## OUTPUT

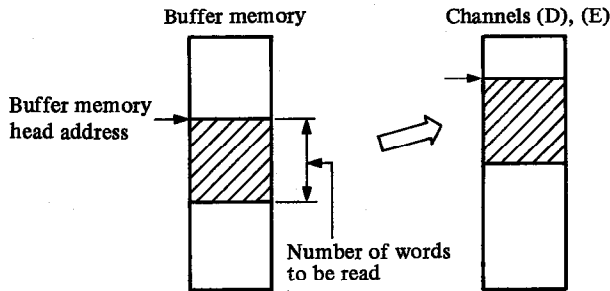
The execution result of SKP is stored into the (H) and (L) registers.

(H), (L) Registers	Contents
0	Normal completion
2	PC access error
8	Buffer memory access error
9	Time out error
10	PC down error
FFFFH(-1)	PC No. error
FFF7H(-9)	Remote error
FFEFH(-17)	Link error

# SR2

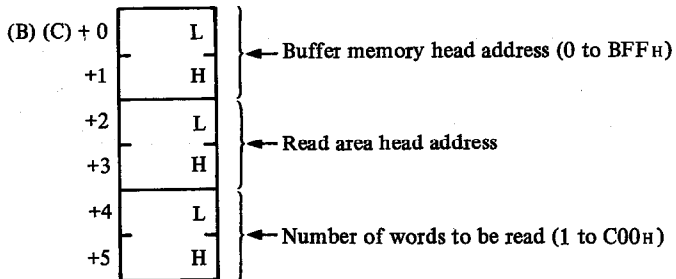
## FUNCTION

Reads data from the buffer memory.



## INPUT

- (D), (E) registers . . . . . Channel which stores the following data
- (B), (C) registers . . . . . Head address of the following data



## OUTPUT

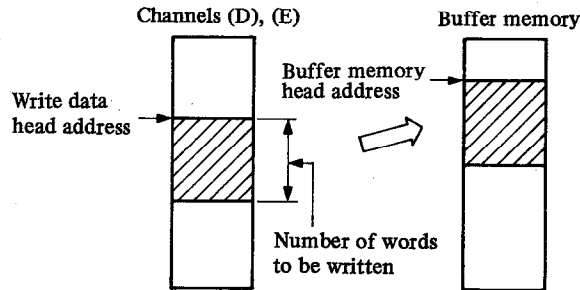
The result is stored into the (H) and (L) registers.

(H), (L) Registers	Judgement
0	Normal completion
1	Channel error
4	Input data error
8	Buffer memory access error

# SW2

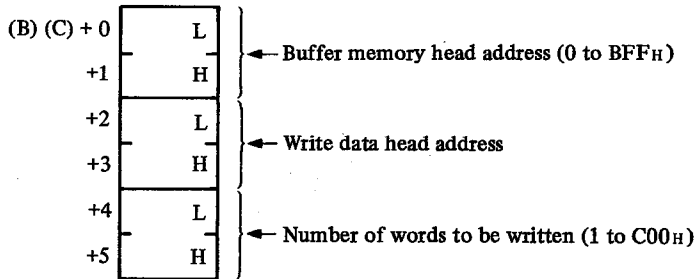
## FUNCTION

Writes data to the buffer memory.



## INPUT

(D), (E) registers . . . . . Channel which stores the following data  
 (B), (C) registers . . . . . Head address of the following data



## OUTPUT

The result is stored into the (H) and (L) registers.

(H), (L) Registers	Judgement
0	Normal completion
1	Channel error
4	Input data error
8	Buffer memory access error

# SADR

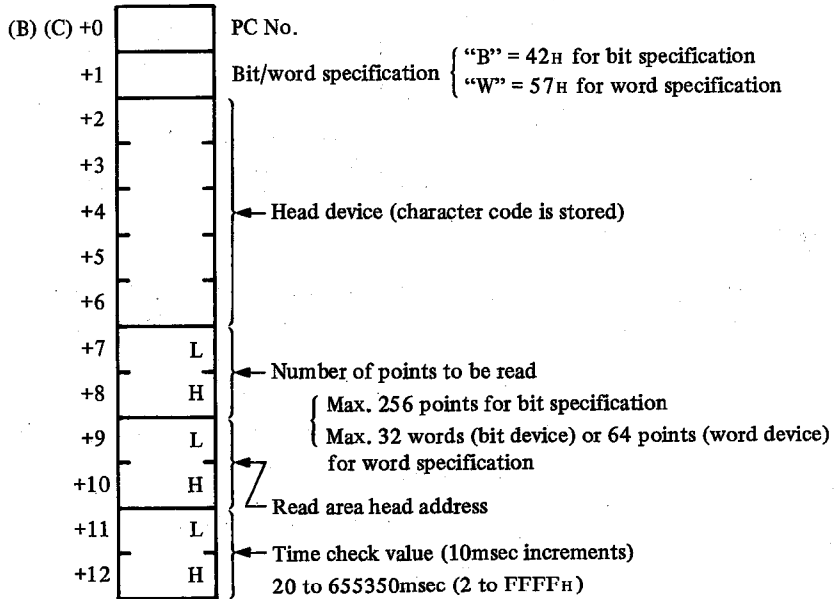
**FUNCTION**

Reads data from the device memory of the PC CPU.

**INPUT**

(D), (E) registers ..... Channel which stores the following setting data

(B), (C) registers ..... Head address of the following setting data



**OUTPUT**

The execution result of SADR is stored into the (H) and (L) registers.

<b>(H), (L) Registers</b>	<b>Judgement</b>
0	Normal completion
1	Channel error
2	PC access error
4	Input data error
8	Buffer memory access error
9	Time out error
10	PC down error
FFFFH(-1)	PC No. error
FFEFH(-17)	Link error

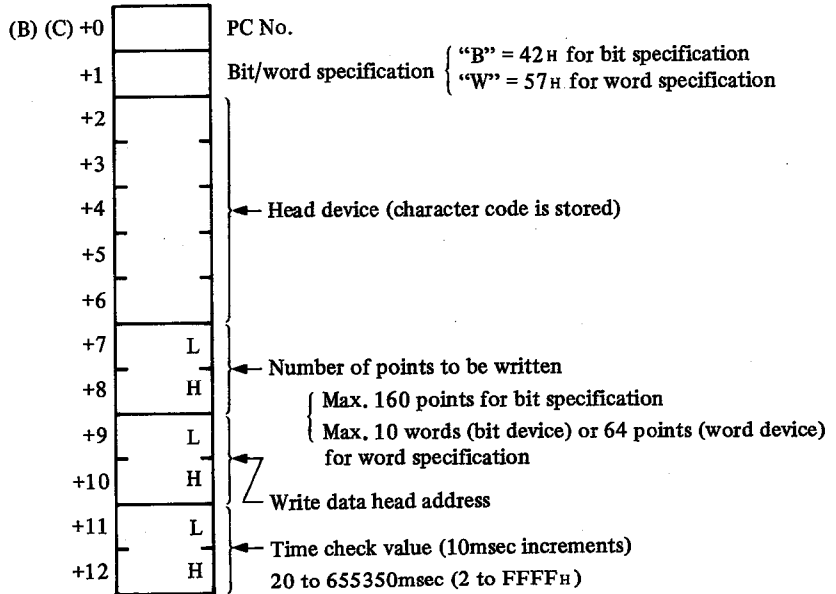
# SADW

## FUNCTION

Writes data to the device memory of the PC CPU.

## INPUT

- (D), (E) registers . . . . . Channel which stores the following setting data  
 (B), (C) registers . . . . . Head address of the following setting data



**OUTPUT**

The execution result of SADW is stored into the (H) and (L) registers.

(H), (L) Registers	Judgement
0	Normal completion
1	Channel error
2	PC access error
4	Input data error
8	Buffer memory access error
9	Time out error
10	PC down error
FFFFH(-1)	PC No. error
FFEFH(-17)	Link error



# SADT

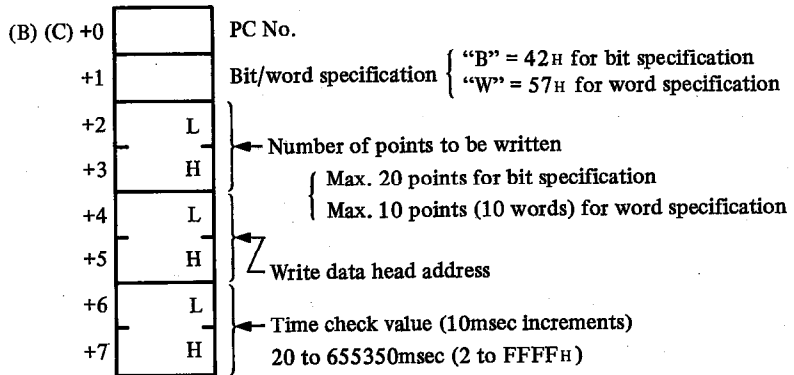
## FUNCTION

Writes randomly specified data to the device memory of the PC CPU.

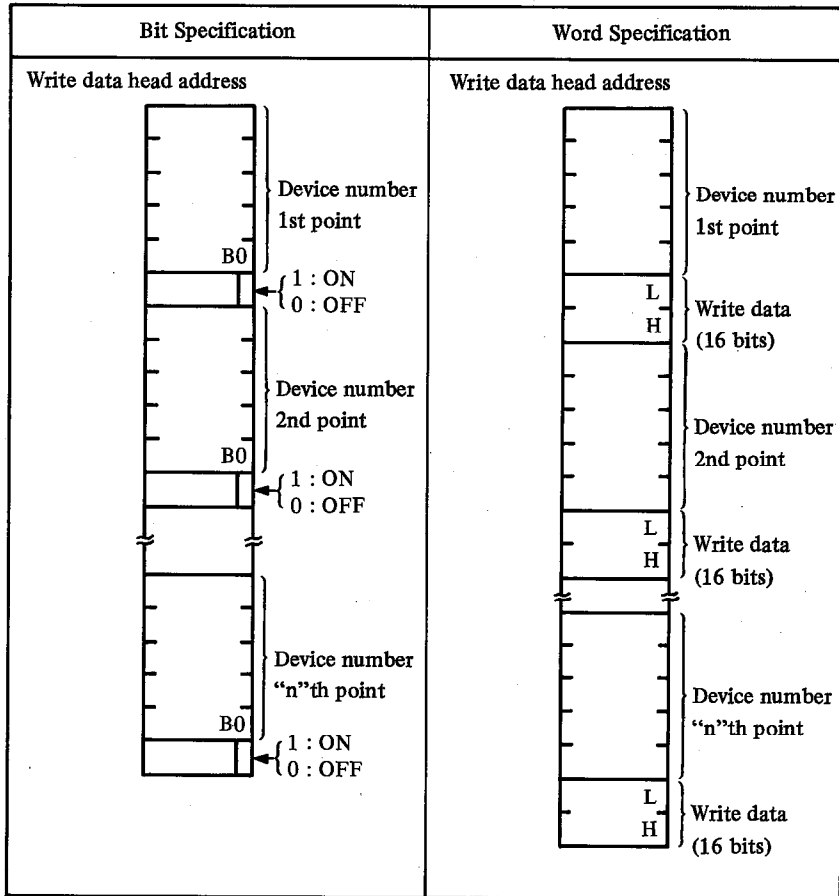
## INPUT

(D), (E) registers ..... Channel which stores the following setting data

(B), (C) registers ..... Head address of the following setting data



Write data format



**OUTPUT**

The execution result of SADT is stored into the (H) and (L) registers.

<b>(H), (L) Registers</b>	<b>Judgement</b>
0	Normal completion
1	Channel error
2	PC access error
4	Input data error
5	Write data error
8	Buffer memory access error
9	Time out error
10	PC down error
FFFFH(-1)	PC No. error
FFEFH(-17)	Link error

# SADMO

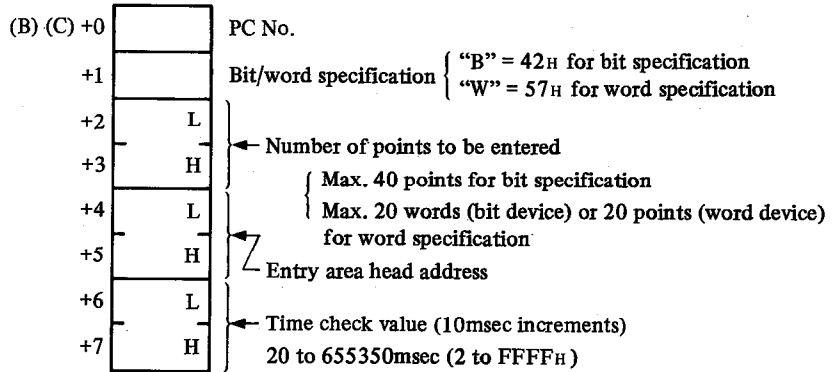
## FUNCTION

Enters a device to be monitored into the AD51.

## INPUT

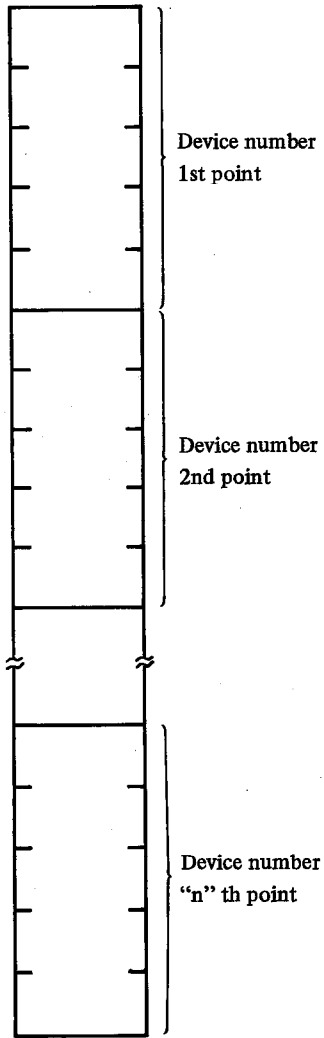
(D), (E) registers . . . . . Channel which stores the following setting data

(B), (C) registers . . . . . Head address of the following setting data



# Entry data format

Entry data head address



**OUTPUT**

The execution result of SADM0 is stored into the (H) and (L) registers.

<b>(H), (L) Registers</b>	<b>Judgement</b>
0	Normal completion
1	Channel error
2	PC access error
4	Input data error
5	Entry data error
8	Buffer memory access error
9	Time out error
10	PC down error
FFFFH(-1)	PC No. error
FFEFH(-17)	Link error

# SADM1

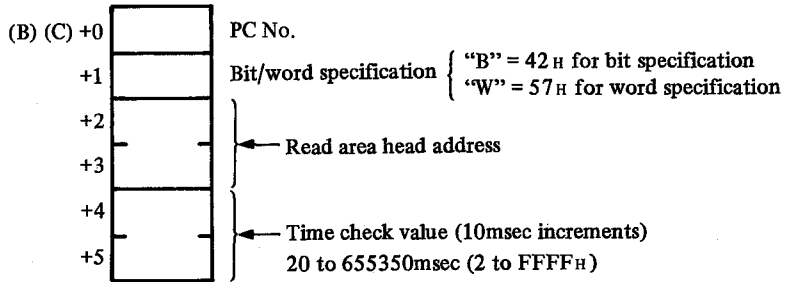
## FUNCTION

Monitors the device entered by monitor data entry (SADM0).

## INPUT

(D), (E) registers . . . . . Channel which stores the following setting data

(B), (C) registers . . . . . Head address of the following setting data



## OUTPUT

The execution result of SADM1 is stored into the (H) and (L) registers.

(H), (L) Registers	Judgement
0	Normal completion
1	Channel error
2	PC access error
4	Input data error
6	No data entered
8	Buffer memory access error
9	Time out error
10	PC down error
FFFFH(-1)	PC No. error
FFEFH(-17)	Link error

# SAAR

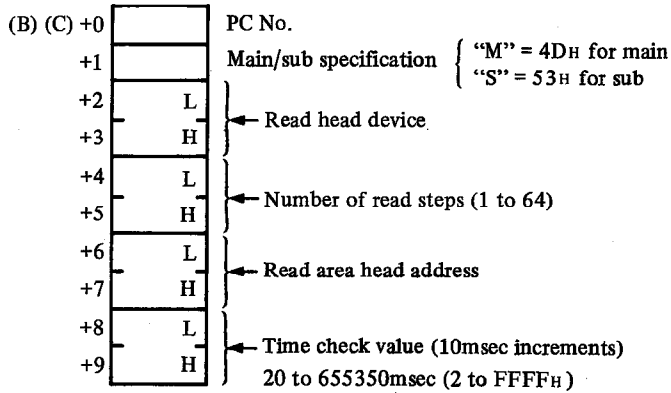
## FUNCTION

Reads a sequence program and T/C set values.

## INPUT

(D), (E) registers . . . . . Channel which stores the following setting data

(B), (C) registers . . . . . Head address of the following setting data



## OUTPUT

The execution result of SAAR is stored into the (H) and (L) registers.

(H), (L) Registers	Judgement
0	Normal completion
1	Channel error
2	PC access error
4	Input data error
8	Buffer memory access error
9	Time out error
10	PC down error
FFFFH(-1)	PC No. error
FFEFH(-17)	Link error
FFFCH(-4)	Other data error



# SAAW

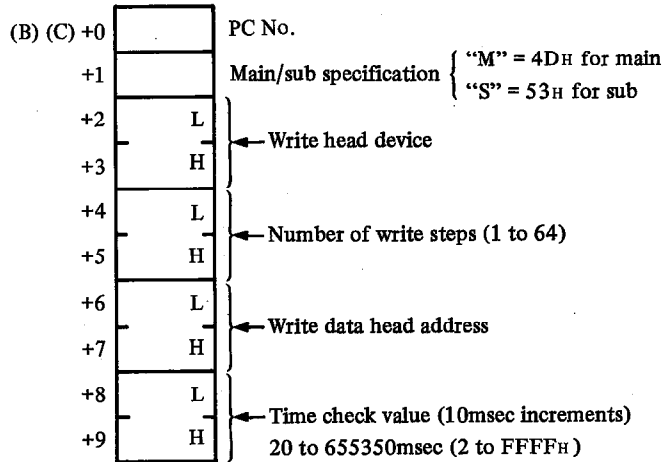
## FUNCTION

Writes a sequence program and T/C set values.

## INPUT

(D), (E) registers . . . . . Channel which stores the following setting data

(B), (C) registers . . . . . Head address of the following setting data



**OUTPUT**

The execution result of SAAW is stored into the (H) and (L) registers.

<b>(H), (L) Registers</b>	<b>Judgement</b>
0	Normal completion
1	Channel error
2	PC access error
4	Input data error
7	Write disable during PC RUN
8	Buffer memory access error
9	Time out error
10	PC down error
FFFFH(-1)	PC No. error
FFFCH(-4)	Other data error
FFEFH(-17)	Link error

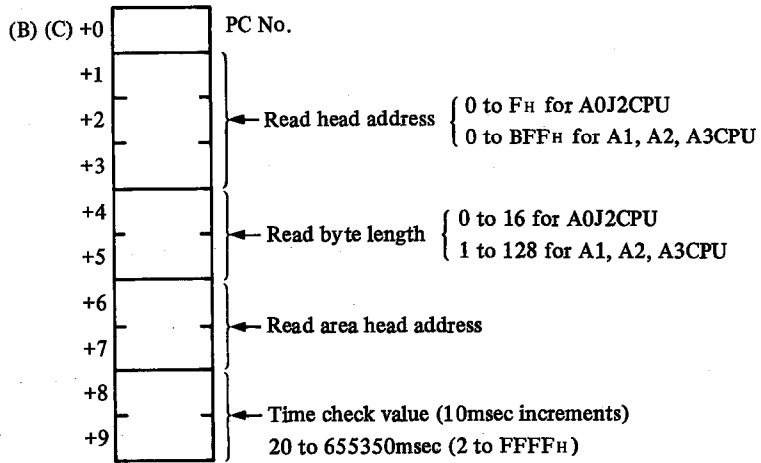
# SAPR

## FUNCTION

Reads parameters from the PC CPU.

## INPUT

- (D), (E) registers . . . . . Channel which stores the following setting data
- (B), (C) registers . . . . . Head address of the following setting data



## OUTPUT

The execution result of SAPR is stored into the (H) and (L) registers.

(H), (L) Registers	Contents
0	Normal completion
1	Channel error
2	PC access error
4	Input data error
8	Buffer memory access error
9	Time out error
10	PC down error
FFFF <sub>H</sub> (-1)	PC No. error
FFEF <sub>H</sub> (-17)	Link error

# SAPW

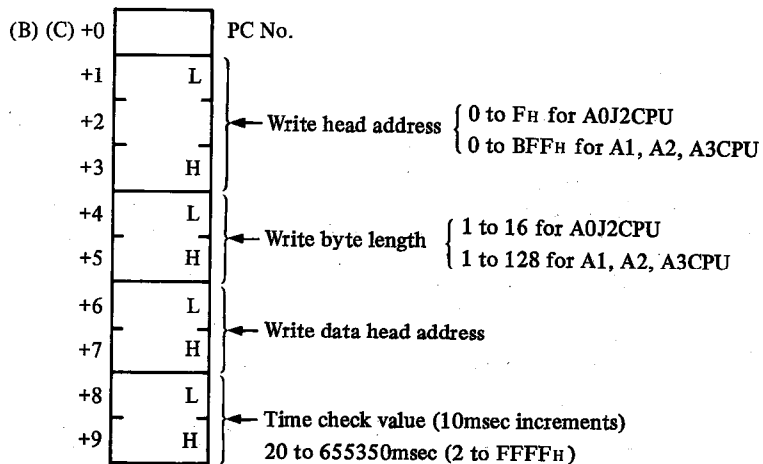
## FUNCTION

Writes data to the parameter area of the PC CPU.

## INPUT

(D), (E) registers . . . . . Channel which stores the following setting data

(B), (C) registers . . . . . Head address of the following setting data



## OUTPUT

The execution result of SAPW is stored into the (H) and (L) registers.

(H), (L) Registers	Contents
0	Normal completion
1	Channel error
2	PC access error
4	Input data error
7	PC RUN
8	Buffer memory access error
9	Time out error
10	PC down error
FFFFH(-1)	PC No. error
FFFCH(-17)	Link error

# SAPS

## FUNCTION

Gives a PC CPU parameter analysis request.

## INPUT

(D), (E) registers . . . . . PC No.  
(B), (C) registers . . . . . Time check value (10msec increments)  
20 to 655350msec (2 to FFFFH)

## OUTPUT

The execution result is stored into the (H) and (L) registers.

(H), (L) Registers	Contents
0	Normal completion
2	PC access error
7	PC RUN
8	Buffer memory access
9	Time out error
10	PC down error
FFFFH(-1)	PC No. error
FFEFH(-17)	Link error

# SIT

## FUNCTION

Interrupts the PC CPU and starts up an interrupt sequence program.

## INPUT

None

## OUTPUT

The execution result of SIT is stored into the (H) and (L) registers.

(H), (L) Registers	Judgement
0	Normal completion of SIT

## NOTE

SIT interrupts the PC CPU, stores 0 into the (H) and (L) registers, and is then complete.

# SIR

## FUNCTION

Reads a currently indicated error and error occurrence entry status among errors displayed at the AD51 indicator.

## INPUT

- (D), (E) registers . . . . . Channel of the area which will store an error flag
- (B), (C) registers . . . . . Head address of the area which will store the error flag

## OUTPUT

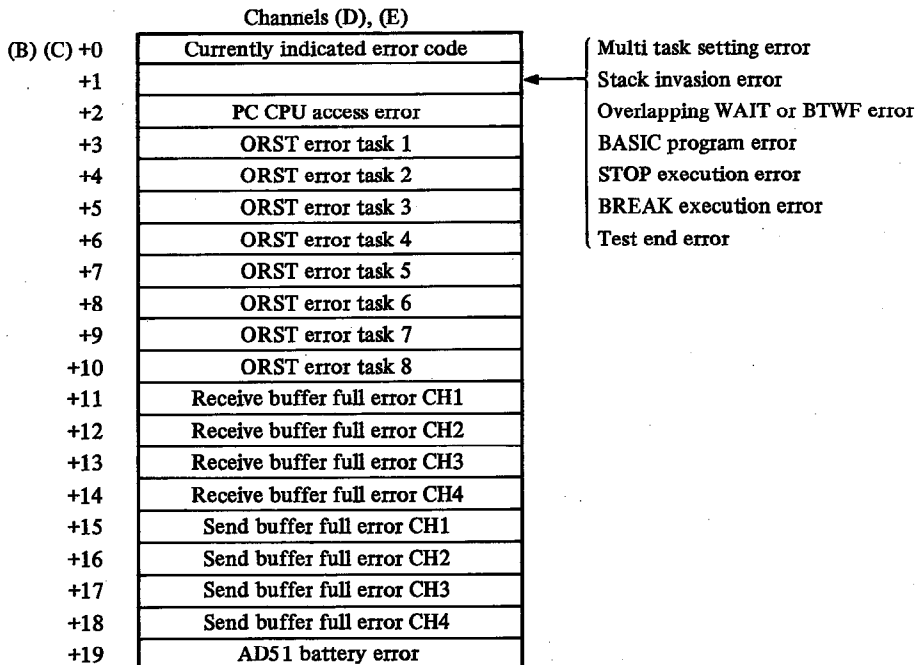
The execution result of SIR is stored into the (H) and (L) registers.

(H), (L) Registers	Judgement
0	Normal completion of SIR
1	Channel error

Upon normal completion, the following data is stored.

When an error exists, the error code is stored in 2-digit BCD.

When an error does not exist, FFH is stored.



# SC2

## FUNCTION

Sets retry time for accessing the buffer memory.

Sets access operation retry time if access cannot be made because the PC CPU is executing the FROM/TO instruction to the AD51.

## INPUT

(D), (E) registers . . . . . Set retry time in the range 0 to 255 (msec).

## OUTPUT

The execution result of SC2 is stored into the (H) and (L) registers.

(H), (L) Registers	Judgement
0	Normal completion of SIR
1	Retry time setting error

## NOTE

At power-on, retry time is set to 10msec.



**IMPORTANT**

**The components on the printed circuit boards will be damaged by static electricity, so avoid handling them directly. If it is necessary to handle them take the following precautions.**

- (1) Ground human body and work bench.**
- (2) Do not touch the conductive areas of the printed circuit board and its electrical parts with any non-grounded tools etc.**

Under no circumstances will Mitsubishi Electric be liable or responsible for any consequential damage that may arise as a result of the installation or use of this equipment.

All examples and diagrams shown in this manual are intended only as an aid to understanding the text, not to guarantee operation. Mitsubishi Electric will accept no responsibility for actual use of the product based on these illustrative examples.

Owing to the very great variety in possible applications of this equipment, you must satisfy yourself as to its suitability for your specific application.

# GPC-BASIC

SUPPLEMENTARY

MODEL	GPC-BASIC-SUP-E
MODEL CODE	13J636
IB(NA)-66100-A(8706)MEE	

 **mitsubishi electric corporation**

HEAD OFFICE : MITSUBISHI DENKI BLDG MARUNOUCHI TOKYO 100-0005 TELEX : J24532 CABLE MELCO TOKYO  
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