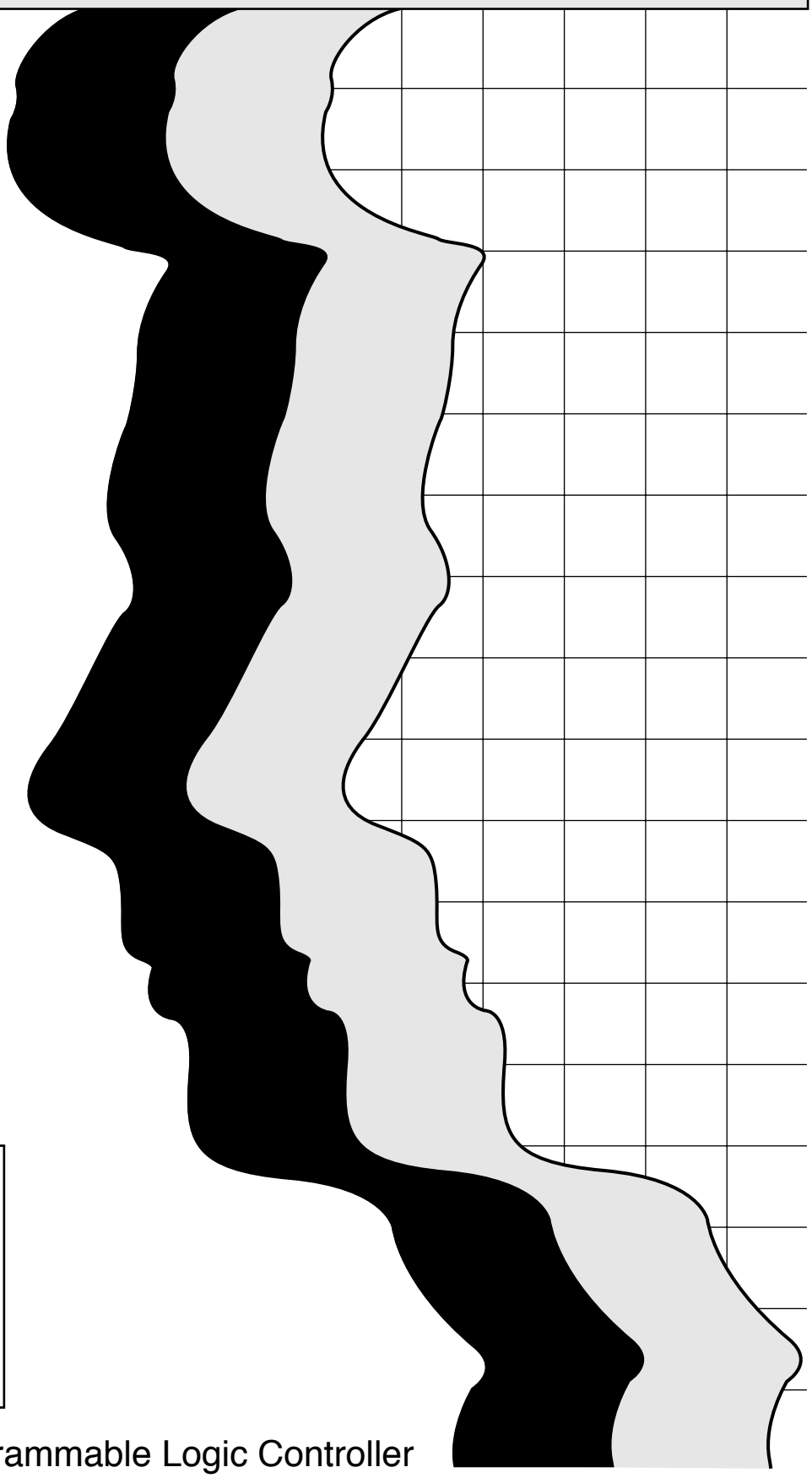
MITSUBISHI

High Speed Counter Module for A0J2 Type A0J2-D61S1

User's Manual



A
MELSEC

Mitsubishi Programmable Logic Controller

● SAFETY PRECAUTIONS ●

(Read these precautions before using.)

When using Mitsubishi equipment, thoroughly read this manual and the associated manuals introduced in this manual. Also pay careful attention to safety and handle the module properly.

These precautions apply only to Mitsubishi equipment. Refer to the CPU module userís manual for a descriprion of the PC system safty precautions.

These ● **SAFETY PRECAUTIONS** ● classifiy the safty precautions into two categories: "DANGER" and "CAUTION".

DANGER	Procedures which may lead to a dangerous condition and cause death or serious injury if not carried out properly.
CAUTION	Procedures which may lead to a dangerous condition and cause superficial to medium injury, or physical damage only, if not carried out properly.

Depending on circumestances, procedures indicated by **CAUTION** may also be linked to serious results.

In many case, it is important to follow the directions for usage.

Store this manual in a safe place so that you can take it out and read it whenever necessary. Always forward it to the end user.

[System Design Precautions]

DANGER

- Safety circuits should be installed external to the programmable controller to ensure that the system as a whole will continue to operate safely in the event of an external power supply malfunction or a programmable controller failure. Erroneous outputs and operation could result in an accident.
  1) Always connect the servo ON signal if the servo amplifier that has the servo ON signal is used. When a servo amplifier which cannot control the stop by the servo ON signal is used, the following processing is necessary.
     - Switch off the power of the PC while the analog voltage is 0 V (while the motor is stopped).
     - Configure the circuit externally so that it turns off ±15 VDC when the PC power is switched off or at the occurrence of a CPU error.

     The analog voltage output (speed command) that is valid immediately before the switching off the power of the PC could be output to cause the motor to run even if the PC power is turned off, the PC CPU is stopped, or the PC CPU error occurs as long as ±15 VDC is applied to the module terminals.
  2) Configure the external interlock circuit, such as emergency stop circuit and upper/lower limits in positioning, that prevents the machine from damage.
  3) The home position return operation is controlled by two sets of data - home position return direction and home position return speed - and deceleration starts in response to the going on of the near-zero point dog signal. Therefore, the motor will keep rotating without decelerated if the direction of home position return is set incorrectly. To protect the machine from troubles occurring due to such nature of the system, it is necessary to configure the measures to protect the machine.

[System Design Precautions]

CAUTION

- Do not bundle control lines or communication wires together with main circuit or power lines, or lay them close to these lines.
  As a guide, separate the lines by a distance of at least 100mm, otherwise malfunctions may occur due to noise.

[Cautions on Mounting]

⚠ CAUTION

- Use the PC in an environment that conforms to the general specifications in the manual.
  Using the PC in environments outside the ranges stated in the general specifications will cause electric shock, fire, malfunction, or damage to/deterioration of the product.
- After installing the module by securely engaging the module fixing projection on the module bottom with the module fixing hole in the base unit, tighten the module clamping screws to the specified torque. Unless the module is installed and screwed correctly, the module can malfunction, fail, or drop.
- Plug in the connectors of the drive unit and peripheral equipment securely to the connectors in the module. Otherwise, loose connection will cause input/output errors.
- Do not touch the conductive areas and electronic parts of the module directly. To do so can cause the module to malfunction or fail.

[Cautions on Wiring]

⚠ DANGER

- Before starting installation, wiring or other work, make sure that the power is switched off externally in all phases.
  Failure to do so may cause an electric shock or damage to the product.
- When starting power-on or operation after installation, wiring or other work, be sure to fit the accessory terminal cover to the product.
  Failure to do so may cause an electric shock.

[Cautions on Wiring]

CAUTION

- Wire the PLC correctly after confirming the rated voltage and terminal arrangement of the product. Failure to do so can cause a fire or failure. Tighten the terminal screws to the specified torque.
- Undertightening can cause a short circuit, fire or malfunction. Overtightening can damage the screws and module, causing the module to fall, short or malfunction.
- Make sure that no foreign matter such as chips or wiring offcuts gets inside the module. It will cause fire, failure or malfunction.
- Crimp or insulation-displace the external connector with the specified tool, or solder it correctly. For the crimping or insulation displacement tool, refer to Chapter 1 of this Userís Manual. Incomplete connection can cause a short circuit, fire or malfunction.

[Cautions on Startup and Maintenance]

DANGER

- Before starting cleaning or terminal screw retightening, be sure to switch power off externally in all phases. Failure to do so can cause an electric shock.

CAUTION

- Do not disassemble or modify any module. This will cause failure, malfunction, injuries, or fire.
- Be sure to install or remove the module after switching power off externally in all phases. Failure to do so can cause the module to fail or malfunction. Undertightening of screws can cause the module to fall, short, or malfunction. Overtightening can damage the screws and module, causing the module to fall, short or malfunction.
- When replacing fuses, be sure to use the prescribed fuse. A fuse of the wrong capacity could cause a fire.
- Before touching the module, be sure to touch ground metal or similar material to discharge static electricity from human body, etc. Failure to do so can cause the module to fail or malfunction.

[Cautions on Disposal]

CAUTION

- Dispose of this product as industrial waste.

CAUTION

MITSUBISHI PROGRAMMABLE CONTROLLER A0J2-D61S1 HIGH-SPEED COUNTER MODULE

On A0J2-D61S1, the count ratios of input pulses are as described below:

(1) Twice for 1-phase input (2 counts are made for 1 pulse input).

(2) Four times for 2-phase input (4 counts are made for 1 pulse input).

For further details, refer to Section 2.2.2 (6) "Counter mode" of the A0J2-D61S1 High-Speed Counter Module User's Manual.

REVISIONS

※The manual number is given on the bottom left of the back cover.

Print Date	*Manual Number	Revision
Nov., 1986	IB (NA) 66094-A	First edition
Dec., 1988	IB (NA) 66094-B	Correction Page 2-1, 2-13, 6-6, 6-13, APP-5, APP-6 "Instructions for Strategic Materials" added
Dec., 2003	IB (NA) 66094-C	Partial Correction CONTENTS, Section 2.2.2, 2.5, 3.1, 4.1.2, 6.1, 6.2, 6.3.1, Appendix 1 Partial Addition Section 2.2.2, 2.5, 4.1.2, 6, 6.1, 6.2, Appendix 1 Addition SAFETY PRECAUTIONS, WARRANTY

INTRODUCTION

Thank you for choosing the Mitsubishi MELSEC-A Series of General Purpose Programmable Controllers. Please read this manual carefully so that the equipment is used to its optimum. A copy of this manual should be forwarded to the end User.

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1. GENERAL DESCRIPTION

This User's Manual describes the A0J2-D61S1 high speed counter module (referred to as "D61S1") giving handling instructions and basic programming information. The D61S1 is used in conjunction with MELSEC-A series programmable controllers.
The D61S1 has 1-phase/2-phase input for two channels and allows counting at maximum 10K/7KPPS.

The following manuals may also be required:

A0J2 User's Manual (CPU unit edition)
A0J2 User's Manual (I/O unit edition)
A0J2CPU Programming Manual
A0J2 Data Link System User's Manual

POINT

In this manual, the D61S1 I/O assignment numbers assume that the unit number is set to 0. If the unit number is other than 0, determine the D61S1 assignment numbers according to the I/O assignment procedure in the Programming Manual.

2. SPECIFICATIONS

This chapter describes the general specifications and performance specifications of the D61S1.

2.1 General Specifications

The general specifications of D61S1 are shown in Table 2.1.

Item	Specifications				
Operating ambient temperature	0 to 55°C				
Storage ambient temperature	−20 to 75°C				
Operating ambient humidity	10 to 90%RH, no condensation				
Storage ambient humidity	10 to 90%RH, no condensation				
Vibration resistance	Conforms to JIS C 0911	Frequency	Acceleration	Amplitude	Sweep Count
		10 to 55Hz	—	0.075mm	10 times *(1 octave/minute)
		55 to 150Hz	1G	—	
Shock resistance	Conforms to JIS C 0912 (10g x 3 times in 3 directions)				
Noise durability	By noise simulator 1500Vpp noise voltage, 1μs noise width and 25 to 60Hz noise frequency				
Dielectric withstand voltage	1500V AC for 1 minute acorss AC external terminals and ground				
Insulation resistance	5MΩ or larger by 500V DC insulation resistance tester across batch of AC external terminals and ground				
Operating ambience	Free of corrosive gases. Dust should be minimal.				
Cooling method	Self-cooling				

Table 2.1 General Specifications

REMARKS

One octave marked * indicates a change from the initial frequency to double or half frequency. For example, any of the changes from 10Hz to 20Hz, from 20Hz to 40Hz, from 40Hz to 20Hz, and 20Hz to 10Hz are referred to as one octave.

2.2 Performance Specifications

The D61S1 is used to count pulses which are occuring at a frequency too high for the CPU counters to use. The D61S1 counts independently of the CPU.

2.2.1 Performance list

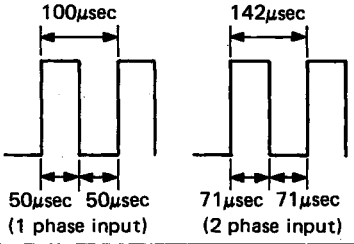
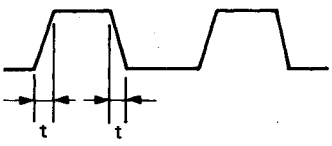
Item			Specifications
			D61S1
I/O points			64 points
Number of channels			2 channels
Performance specifications of 1 channel	Count input signal	Phase	1 phase input, 2 phase input
		Signal level (Phase A, Phase B)	5V DC, 12V DC, 24V DC } 2 to 5mA
	Counter	Counting speed *(Maximum)	1 phase input: 10KPPS 2 phase input: 7KPPS
		Counting range	24 bits binary 0 to 16,777,215 (decimal)
		Form	Up/down preset counter plus ring counter function
		Minimum count pulse width (Set input rise and fall times to 5μs. or less. Duty ratio: 50%)	
	Magnitude comparison between CPU and D61S1	Comparison range	24 bits, binary
		Comparison result	Set value < count value Set value = count value Set value > count value
	External input	Preset	12/24V DC, 3/6mA 5V DC, 5mA
		Count disable	12/24V DC, 3/6mA 5V DC, 5mA
	External output	Coincidence output	Transistor (open collector) output 12/24V DC, 0.5A
Current consumption			5V DC, 0.1A
Weight			0.65kg

Table 2.2 Performance List

*: Counting speed is influenced by pulse rise time and fall time. Countable speeds are as follows.

Rise/Fall Time	1 Phase Input	2 Phase Input
t = 5μs or less	10KPPS	7KPPS
t = 500μs	500PPS	250PPS



If the rise or fall time is more than 500μs, miscount may occur. Use the D61S1 at 500μs or less.

2.2.2 Functions

This section explains the functions of the D61S1.

(1) General description

The D61S1 unit counts high-speed pulse input which cannot be used directly of programmable controller CPU.
D61S1 incorporates a BIN (binary) 24-bit preset counter function which is capable of up/down count, a ring counter function, an internal preset function, an external disable function, a comparison function with BIN 24-bit set value, and a coincidence signal external output function, applicable to two channels.

(2) Block diagram

The following shows the block diagram of the D61S1.

General operation

CH1 counter counts the pulse train entering its phase A input up or down as appropriate. In order to read a count value from the CPU unit, it is necessary to read the value via the buffer memory. I/O signals to and from the programmable controller CPU are used to control the operation of the counter. The buffer memory is used to store set data, etc. which controls the counter.

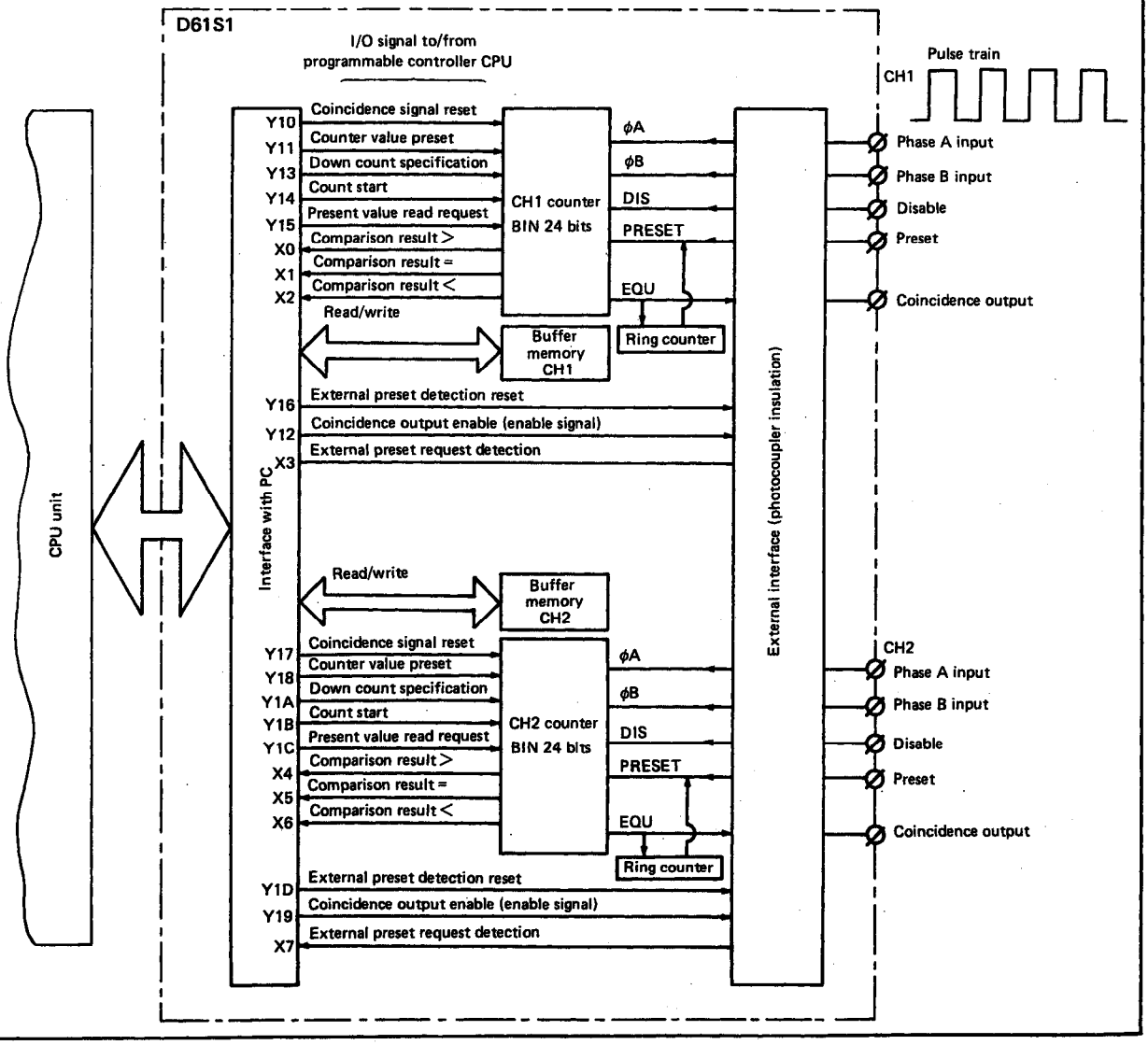
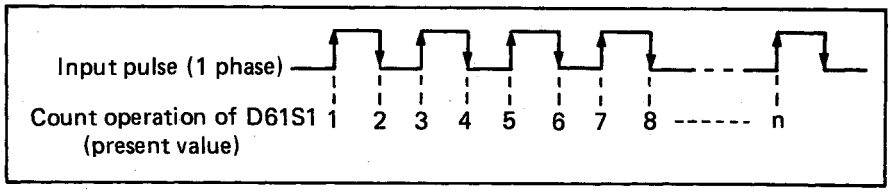


Fig. 2.1 Block Diagram

(3) General description

The D61S1 counts the number of input pulses. In the following figure, for example, each time a pulse is input, the D61S1 counts pulses in order of 1 to 2 to 3 to 4 to n. The D61S1 high-speed counter is capable of accepting an input pulse speed of 10KPPS (7KPPS for 2 phases). The allowable counting range is 0 to 16,777,215. The D61S1 unit always executes the comparison function (>, =, <) with a set value (a target value optionally set by user).



(4) Pulse input

Pulse inputs may be 1-phase or 2-phase. For 1-phase pulse input, up count (down count specification is also possible from the main program) is made each time a pulse is input. For 2-phase pulse input, the up/down direction of the counter is automatically judged depending on the relation between phase A and phase B. In the following figure, the voltages at the D61S1 count input terminal are shown for 1-phase and 2-phase inputs. In this manual, explanation will be given in reference to source load.

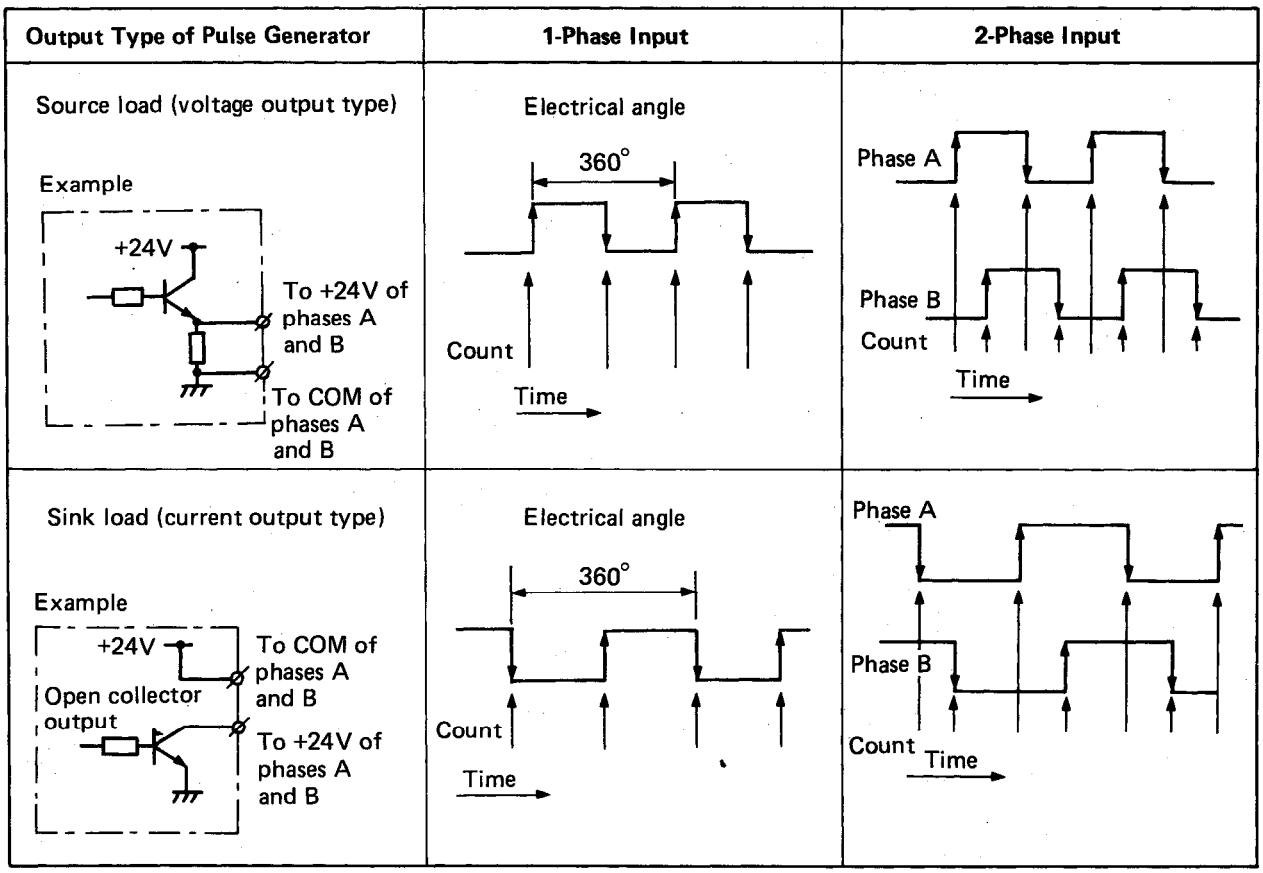


Fig. 2.2 1-Phase and 2-Phase Inputs

(5) Count timing

The timing (for 1 phase input) of the comparison result between a present value and a set value is as indicated below. (Indicated by the assignment numbers of CH1 and 2.)

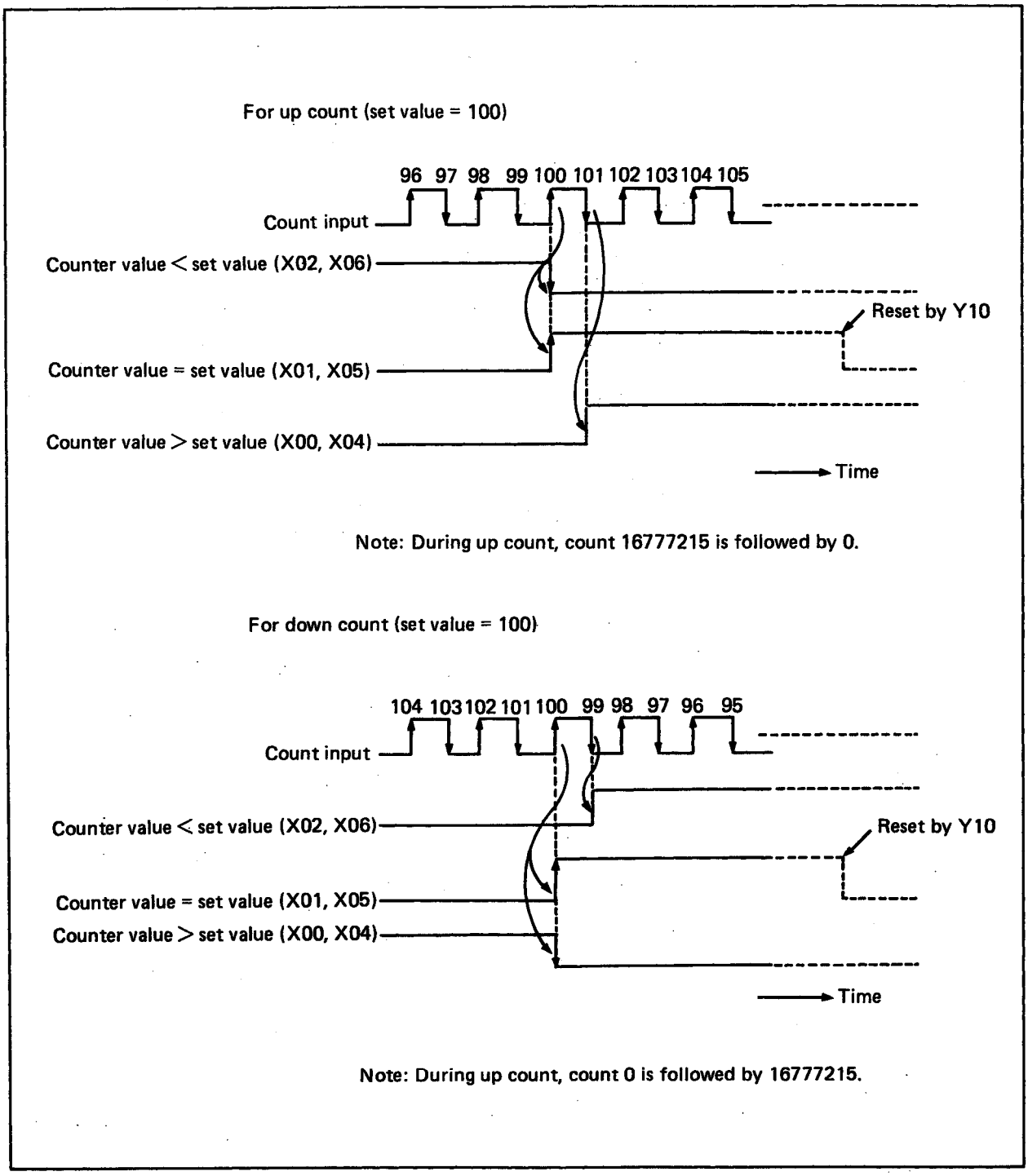


Fig. 2.3 Count Timing

(6) Count mode

On D61S1, the count rations of input pulses are as described below:

1) Twice for 1-phase input (2 counts are made for 1 pulse input).
2) Four times for 2-phase input (4 counts are made for 1 pulse input).

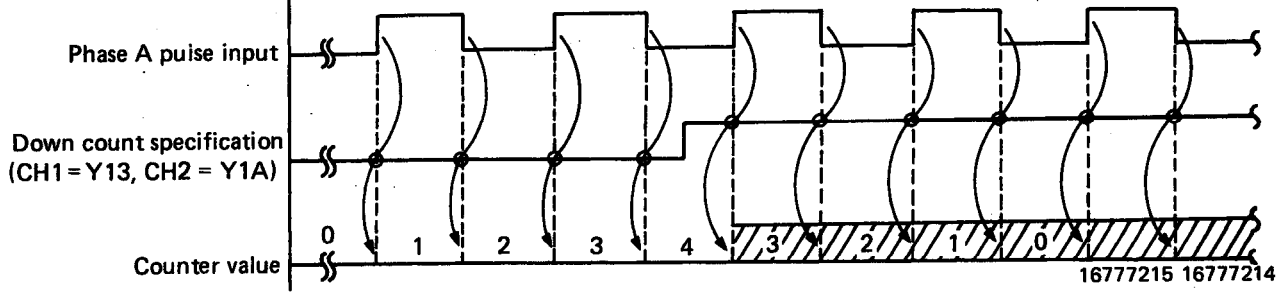
POINT

1. **Each input pulse registers two counts for 1-phase input and four counts for 2-phase input. If the counting range is large, select the pulse generator so that a value twice (for 1 phase) or four times (for 2 phases) greater than the number of generated pulses is within the counting range (0 to 16,777,215).**

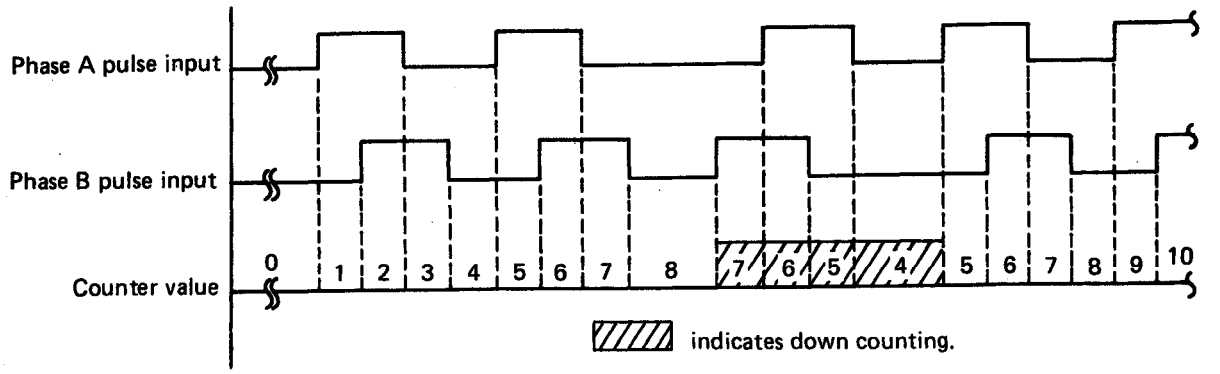
2. **For 1-phase input, specify any set value as twice the actual number of input pulses or halve the present value (by using D/instruction). For 2-phase input, specify any set value as four times the actual number of input pulses or divide the present value by four (by using D/instruction).**

Counting methods for 1-phase input and 2-phase input are shown below. When 1 phase is used, down counting is made if down count specification is on. When 2 phases are used, down count is made if phase B input pulse leads phase A input pulse.

Count timing when 1 phase is used



Count timing when 2 phases are used



(7) Preset function

When the power to the D61S1 is turned off, or the CPU reset, the D61S1 memory contents are lost (i.e. present values, set values etc.). If these values need to be retained for subsequent use, they must be stored in a suitable data register in the Programmable controller CPU.

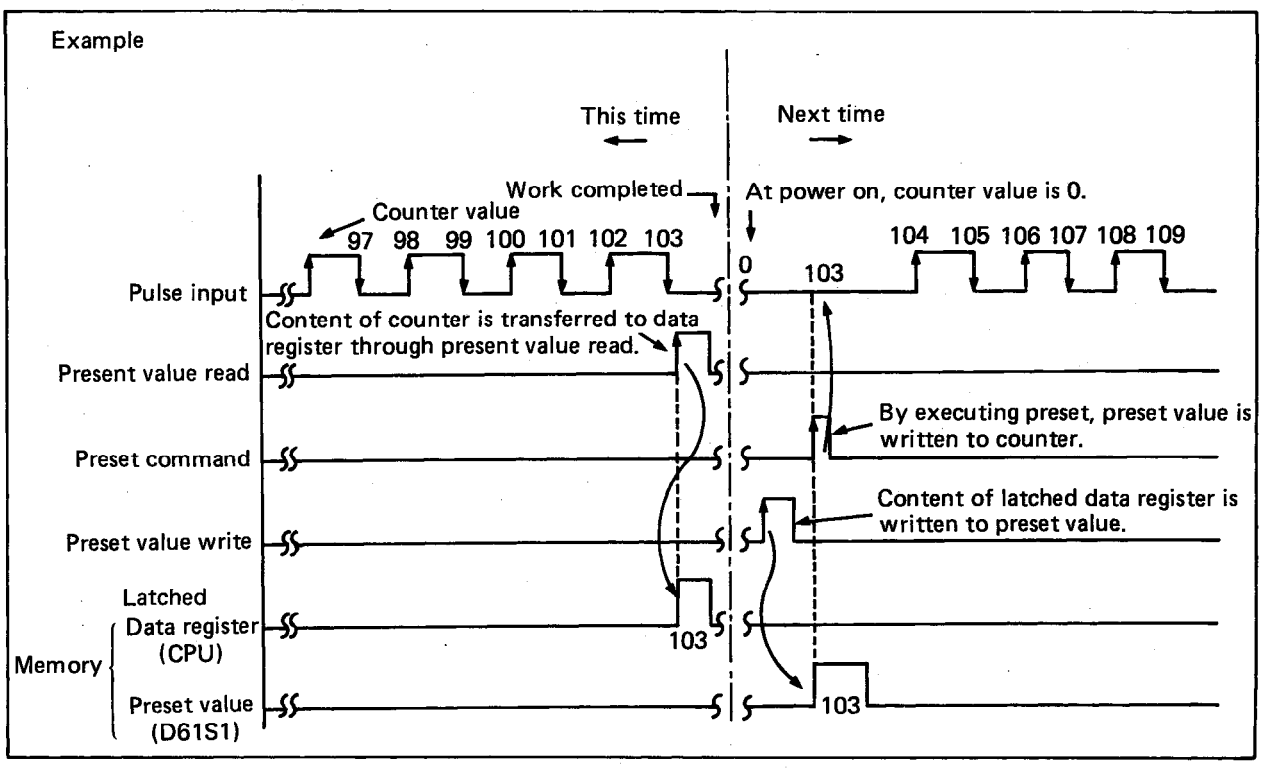


Fig. 2.4 Preset Operation

- The preset value is written to the appropriate buffer memory address (address 1 for CH1, address 33 for CH2) as a 24 bit binary number.
  To load the preset value into the counter current value turn on the preset command (Y 11 for CH1, Y18 for CH2) from the programmable controller CPU.

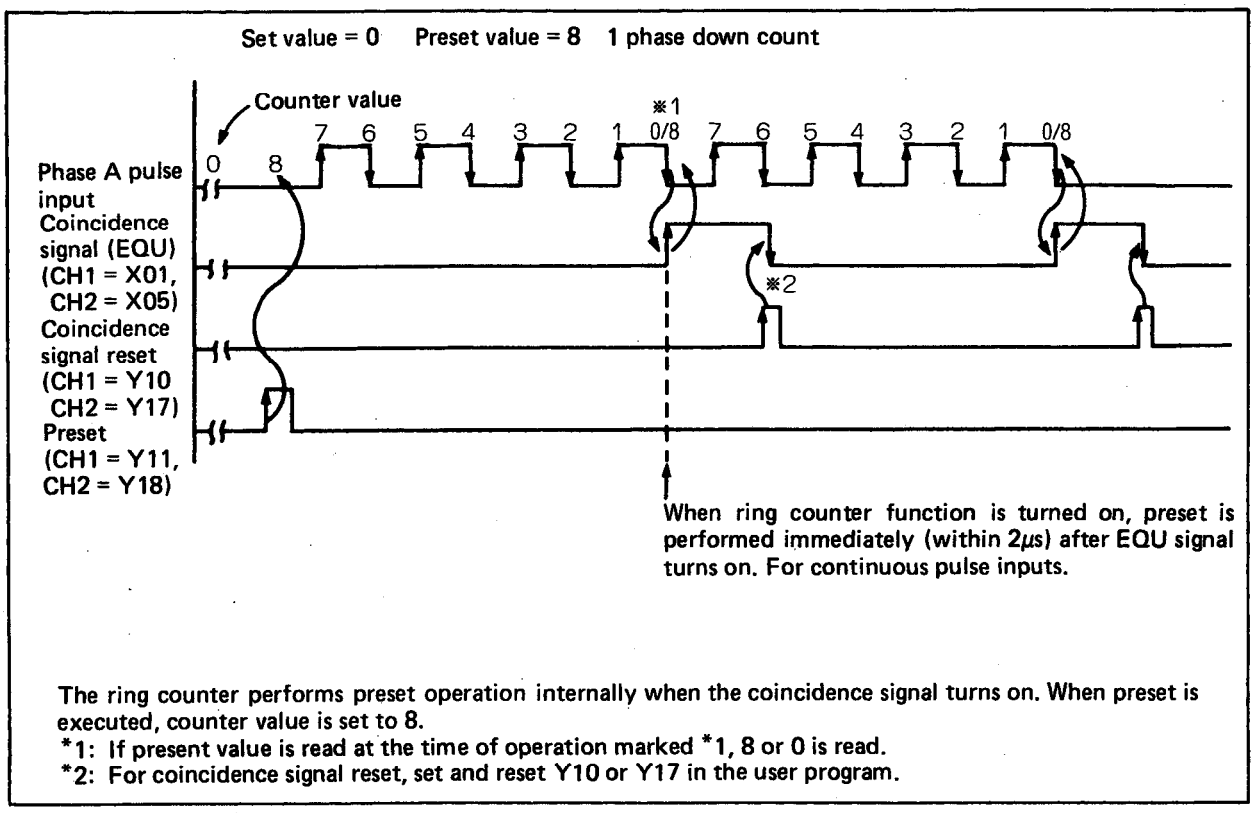
- The preset command may either be loaded from the program or input by applying a voltage to the PRST terminal on the external terminal block (external preset).
  When the external preset signal is given, a flip flop (F/F) is set. If the external preset input turns on again while the F/F is set, the presetting function is stopped. Reset the F/F from the program. (Y16 for CH1, Y1D for CH2) Even if the external preset input remains on, the F/F can be reset. (The F/F is set on the leading edge of the external preset pulse.)

(8) Disable function

By turning on the count enable signal (i.e. a programmable controller I/O signal), D61S1 starts counting. (Y14 for CH1, Y1B for CH2)
When a voltage is applied to the DIS (disable) terminal on the external input terminal block, the D61S1 stops counting. By utilizing this, counting may be started and stopped by the external input, irrespective of scan time.

(9) Ring counter function

By setting the ring counter setting switch on the D61S1 circuit board to ON position, automatic preset is performed if the counter value becomes equal to the set value. Use this function for cyclic control such as sizing feed. The timing for the ring counter is shown below.



The ring counter performs preset operation internally when the coincidence signal turns on. When preset is executed, counter value is set to 8.
*1: If present value is read at the time of operation marked *1, 8 or 0 is read.
*2: For coincidence signal reset, set and reset Y10 or Y17 in the user program.

Fig. 2.5 Ring Counter Operation

(10) External output

D61S1 is capable of giving a counter value coincidence signal (open collector output) (which turns on if the counter value is equal to the set value). In order to use the counter coincidence signal, it is necessary to turn on the coincidence signal output enable (Y12 for CH1, Y19 for CH2) which is assigned to the programmable controller I/O.

2.3 I/O Signals To and From Programmable Controller CPU

This section describes I/O signals to and from programmable controller CPU when the D61S1 unit number is set to 0.

	CH1	CH2	Signal	Description
Input signal	X00	X04	Counter value greater	Turned on if counter value is greater than set value.
	X01	X05	Counter value coincidence	Latched on if counter value is equal to set value. Turned off by coincidence signal reset command.
	X02	X06	Counter value less	Turned on if counter value is less than set value.
	X03	X07	External preset request detection	Latched on when preset request is given from external input. Turned off when external preset detection signal is reset.

Table 2.3 Input Signals

- Do not use X08 to X0F signals.
- Counter value coincidence signal is turned on when the power is turned on or reset is executed because both the counter value and set value are 0. Therefore, always reset the counter coincidence signal first by turning the coincidence signal reset command on and then off.
- If the counter and set values are still the same after executing the coincidence signal reset command, the counter value coincidence signal is enabled again.

	Channel		Signal	Operation Timing	Description
	CH1	CH2			
Output signal	Y10	Y17	Coincidence signal reset command		Reset signal for counter value coincidence signal (latch) and coincidence output (EQU) signal
	Y11	Y18	Preset command		Preset value write execution signal
	Y12	Y19	Coincidence signal output enable		By turning on this signal, counter value coincidence signal is output to outside.
	Y13	Y1A	Down count command		If this signal is on in 1 phase mode, down count is performed.
	Y14	Y1B	Count enable		By turning on this signal, count operation is enabled.
	Y15	Y1C	Present value read request		At the rise of this signal, count value is read as present value.
	Y16	Y1D	External preset detection reset command		Reset signal of external preset request detection signal (latch)

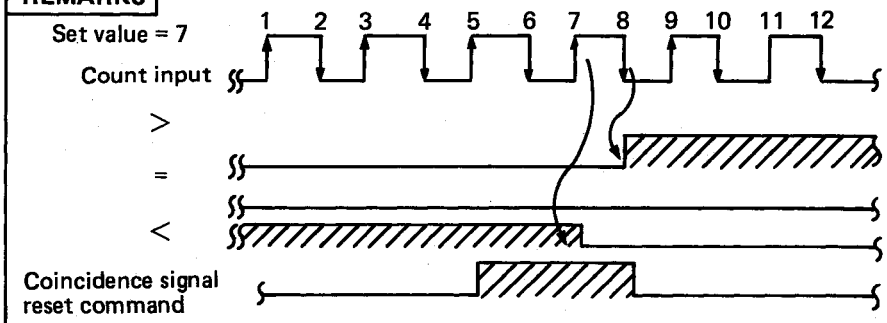
Table 2.4 Output Signals

IMPORTANT

Y00 to 0F and Y1E to 1F may not be used as they are reserved. If one of the above signals is used (turned on/off) in a sequence program, the functions of the D61S1 cannot be graranteed. However, when the D61S1 is used for remote I/O, Y0E and Y0F may be reset from the program. (For details, refer to Section 6.3.)

- In Table 2.4 the symbol ⌐¬ indicates that the function is executed on the rise of the signal.
- The coincidence signal latches itself on and must be reset from the sequence program.

REMARKS

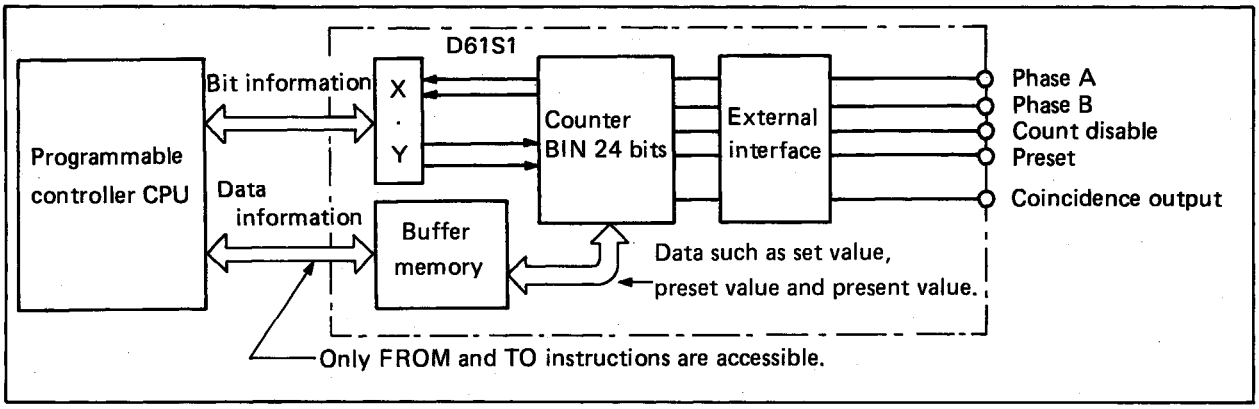


- The external preset detection reset command must be executed at high speed so that the scan time of the program has mininal effect on the D61S1 operation.
  For this reason use a SET Y16 instruction followed by RST Y16, this is fully explained later in this manual.

2.4 Buffer Memory

(1) General description

By using FROM and TO instructions, the D61S1 is capable of making data communication with the programmable controller CPU through the buffer memory.



(2) Memory map

The memory map inside the buffer memory is shown below. When the power is turned on or the CPU is reset, the contents of the buffer memory are initialized to 0. Preset value, present value, and set value are handled as 24 bit binary. (The address consists of 16 bits and expressed in decimal.)

CH1 address	CH2 address		
1	33	Preset value write (lower and middle)	Write only
(2)	(34)	Preset value write (upper)	
3	35	Mode register	Read/write
4	36	Present value read (lower and middle)	Read only
(5)	(37)	Present value write (upper)	
6	38	Set value read/write (lower and middle)	Read/write
(7)	(39)	Set value read/write (upper)	

Addresses in parentheses in the above table indicate those of the upper 8 bits of 24-bit data.

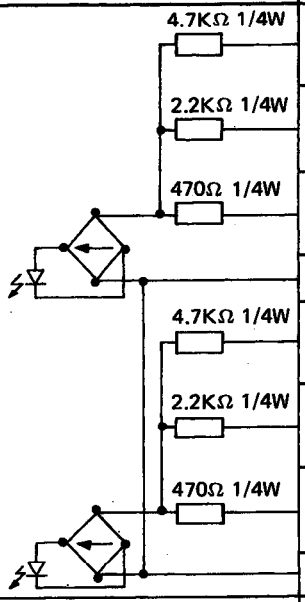
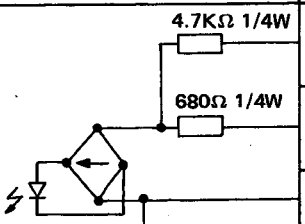
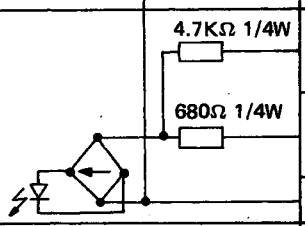
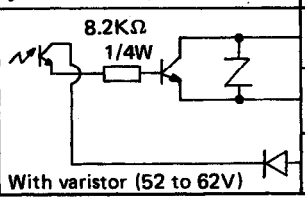
(3) Setting of mode register

Set the value of the mode register as indicated in the following table. The value is indicated in decimal.
When the power is turned on, the value is 0.

Division of Phase	Data to Be Written
1 phase	8
2 phases	18

2.5 Interface with External Equipment

The external equipment interface list of D61S1 is indicated below.

I/O Division	Internal Circuit	Terminal Number CH1	Terminal Number CH2	Signal	Operation	Input Voltage (Guaranteed value)	Operation Current (Guaranteed value)
Input		1	19	Phase A pulse input 24V	At ON	21.6 to 26.4V	2 to 5mA
					At OFF	5V or less	0.1mA or less
		2	20	Phase A pulse input 12V	At ON	10.8 to 13.2V	2 to 5mA
					At OFF	4V or less	0.1mA or less
		3	21	Phase A pulse input 5V	At ON	4.5 to 5.5V	2 to 5mA
					At OFF	2V or less	0.1mA or less
		4	22	COM			
		5	23	Phase B pulse input 24V	At ON	21.6 to 26.4V	2 to 5mA
					At OFF	5V or less	0.1mA
		6	24	Phase B pulse input 12V	At ON	10.8 to 13.2V	2 to 5mA
					At OFF	4V or less	0.1mA or less
		7	25	Phase B pulse input 5V	At ON	4.5 to 5.5V	2 to 5mA
					At OFF	2V or less	0.1mA or less
		8	26	COM			
Input		9	27	Disable input 12/24V	At ON	10.2 to 26.4V	2 to 6mA
					At OFF	2V or less	0.1mA or less
		10	28	Disable input 5V	At ON	4.5 to 5.5V	3.5 to 5.5mA
					At OFF	1.5V or less	0.1mA or less
		11	29	COM	Response time	OFF → ON 0.5ms or less	ON → OFF 3ms or less
Input		12	30	Preset input 12/24V	At ON	10.2 to 26.4V	2 to 6mA
					At OFF	2V or less	0.1mA or less
		13	31	Preset input 5V	At ON	4.5 to 5.5V	3.5 to 5.5mA
					At OFF	1.5V or less	0.1mA or less
		14	32	COM	Response time	OFF → ON 0.5ms or less	ON → OFF 3ms or less
Output		15	33	Open collector output OUT	Operating voltage: 10.2 to 30V Rated voltage: 0.5A Maximum rush current: 4A, 10msec Maximum voltage drop at ON: 1.5V at 0.5A Response time: OFF → ON 0.1msec or less (Resistor load) ON → OFF 0.1msec or less		
		16	34	0V			
		17	35	12/24V external power input	Input voltage: 10.2 to 30V Current consumption: 2 to 5mA		

REMARKS

The AD61 accepts encoders in open collector output system and CMOS output system. Encoders in TTL output system and line driver output system are unavailable. When using an encoder in CMOS output system, check whether the output voltage of the encoder conforms to the D61S1 specifications.

3. HANDLING

This chapter describes the handling instructions, nomenclature, maintenance, and inspection of the D61S1.

3.1 Handling Instructions

(1) Protect the D61S1 and its terminal block from impact.

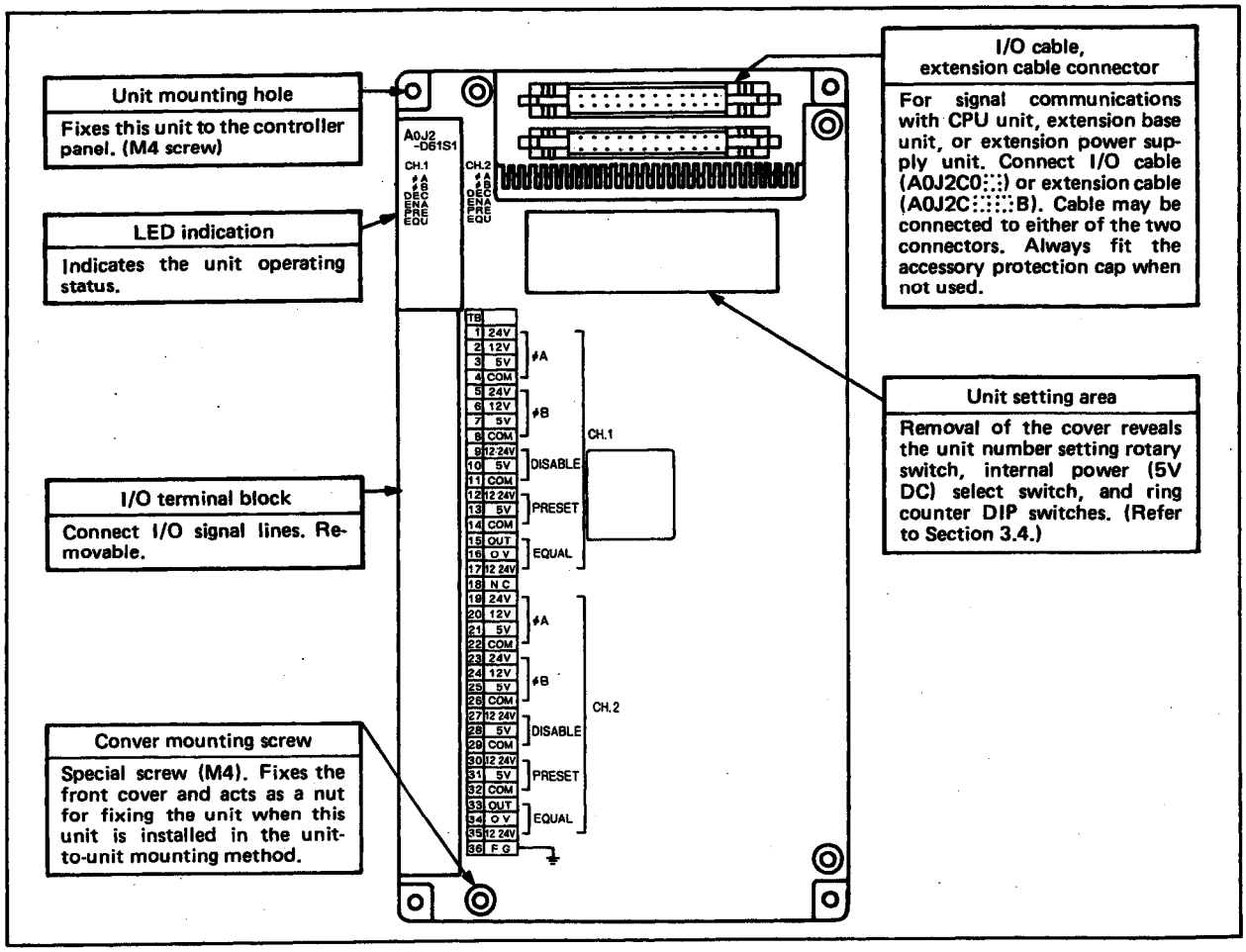
(2) Do not touch or remove the printed circuit board from the case.

(3) When wiring, ensure that no wire offcuts enter the unit and remove any that do enter.

(4) Tighten terminal screws as specified below.

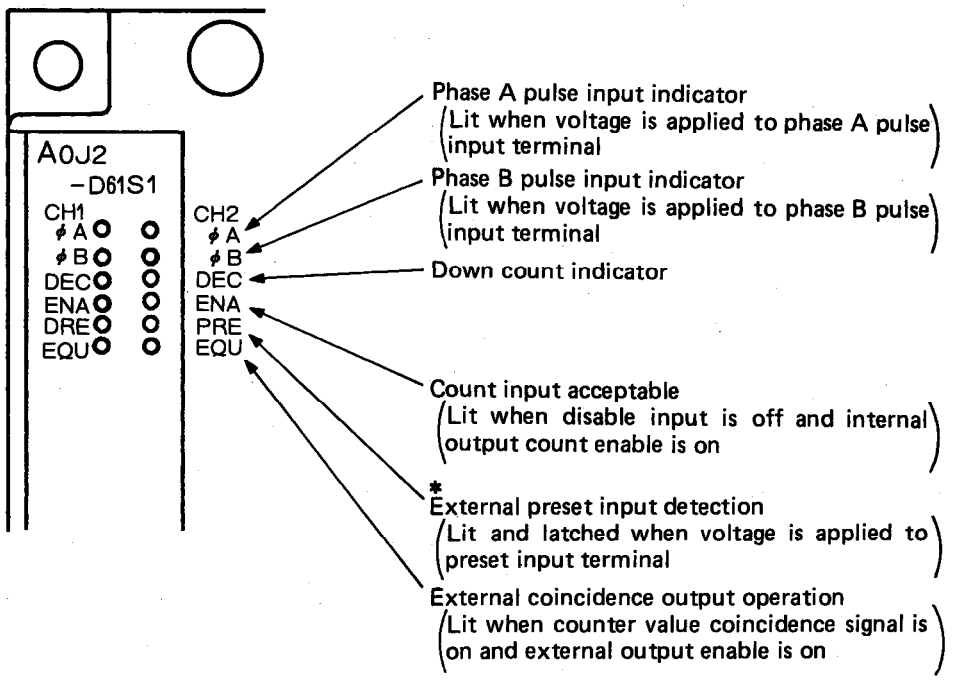
Screw Location	Tightening Torque Range
I/O terminal block terminal screw (M3 screw)	49 to 78 N·m
I/O terminal block mounting screw (M4 screw)	78 to 137 N·m
Unit mounting screw (M4 screw)	78 to 117 N·m

3.2 Nomenclature and Explanation



3.3 LED Indicators

LED "on" conditions are explained below. LED operations of CH1 are the same as those of CH2.



REMARKS

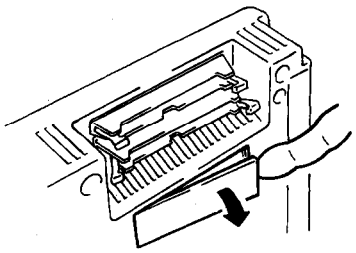
*If external preset detection reset signal (Y16 for CH1, Y1D for CH2) is turned on when this LED is on, it will turn off.

3.4 Unit Setting Area Settings

3.4.1 Unit number setting

This section describes unit number setting.

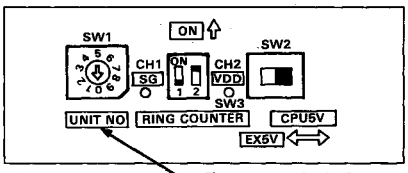
Remove the cover of unit setting area from the unit as shown on the right.



Select and set one of 0 to 7 with the unit number (UNIT NO) setting rotary switch. (Using a screwdriver)

Install the cover of unit setting area to the unit.

Completed



	Unit Number Setting							
	0	1	2	3	4	5	6	7
Unit number rotary switch setting								

POINT

(1) Set the rotary switch for unit number setting to an appropriate number in the range 0 to 7 according to the number of unit. Note that setting the same unit number between units causes input/output errors.

(2) Setting of unit number determines X and Y addresses. For details, refer to Section 5.1 and 5.2.

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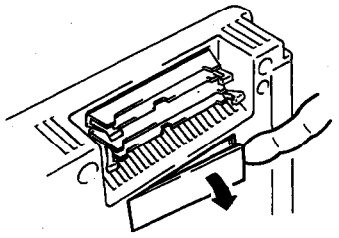
3.4.2 Ring counter function setting

Remove the unit setting area cover from the unit as shown on the right.

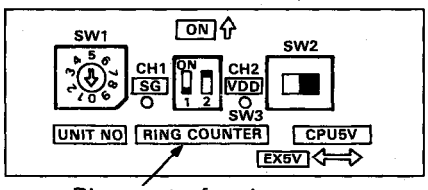


Set whether the ring counter function is used or not with the RING COUNTER setting DIP switches. (When using the function, set to ON. When not using the function, set to OFF.)

Install the setting area cover to the unit.

Completed

Inside the unit



Ring counter function setting DIP switches

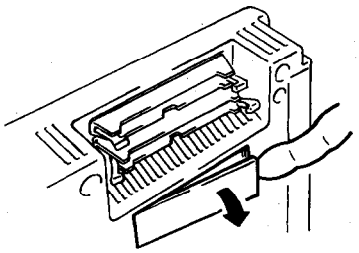
	Ring Counter Function Setting				
CH1	Unused	Used	Unused	Used	
CH2	Unused	Unused	Used	Used	
Ring counter setting switches					

*Black area indicates the slide switch position.

3.4.3 Unit internal power supply (5V DC) setting

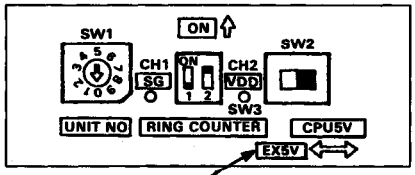
This section describes the setting of unit internal power supply (5V DC).

Remove the cover of unit setting area from the unit as shown on the right.



Check and set the unit internal power supply (5V DC) select switch. Set to "CPU5V" when the power is supplied by the CPU unit built-in power supply, and to "EX5V" when supplied from the extension power supply unit.

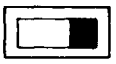
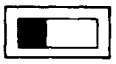
Inside the unit



Install the cover of unit setting area to the unit.

Completed

I/O unit internal power supply (5V DC) select switch

	Unit Internal Power Supply (5V DC) Setting	
	Power supplied from CPU unit built-in power supply	Power supplied from extension power supply unit
Unit internal power supply (5V DC) select switch	 EX5V ◄——► CPU5V	 EX5V ◄——► CPU5V

*Black area indicates the slide switch setting position.

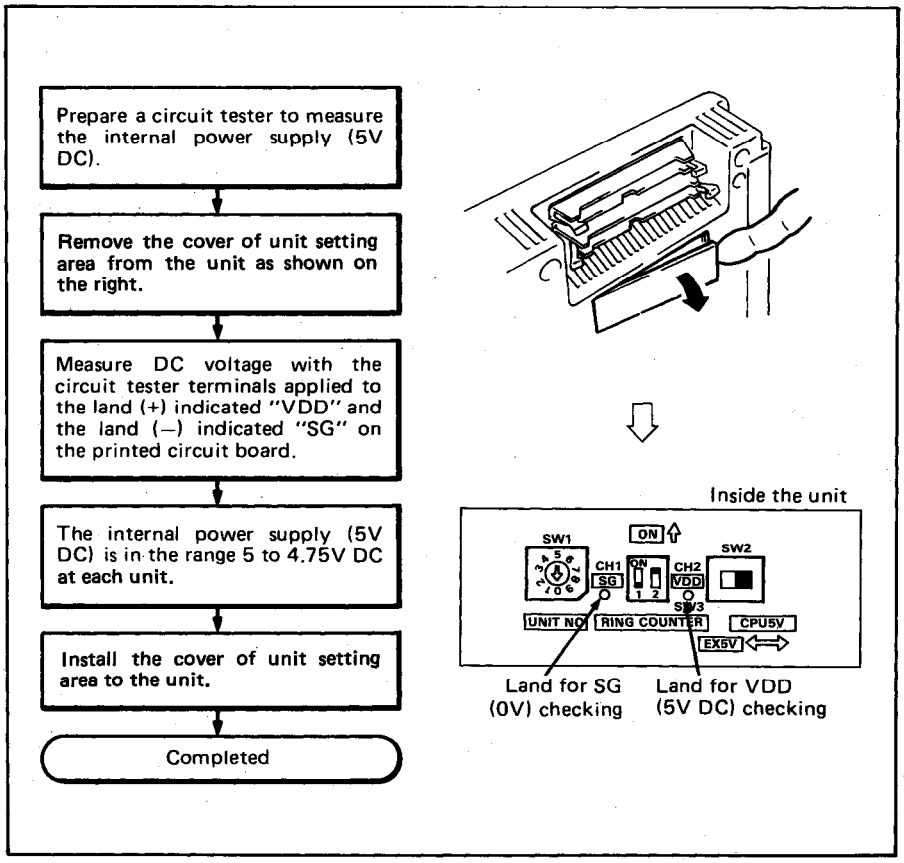
POINT

(1) If the select switch is set to EX5V when unit is supplied with 5V DC power by the CPU unit internal power supply, the unit does not operate properly. Be sure to check before the trial run.

(2) To set the system using Type A0J2PW extension power supply unit, refer to the A0J2 CPU User's Manual (CPU Unit Edition).

3.4.4 Unit internal power supply (5V DC) check

This section describes how to check the unit internal power supply (5V DC). Use a circuit tester for measurement.



POINT

The following switches are factory-set as described below:

Unit number setting switch 0
Ring counter function setting switch. . . . .
. . . . . .OFF (function unavailable) for CH1 and 2
Internal power setting switch . . . . . .CPU

4. WIRING AND INSTALLATION

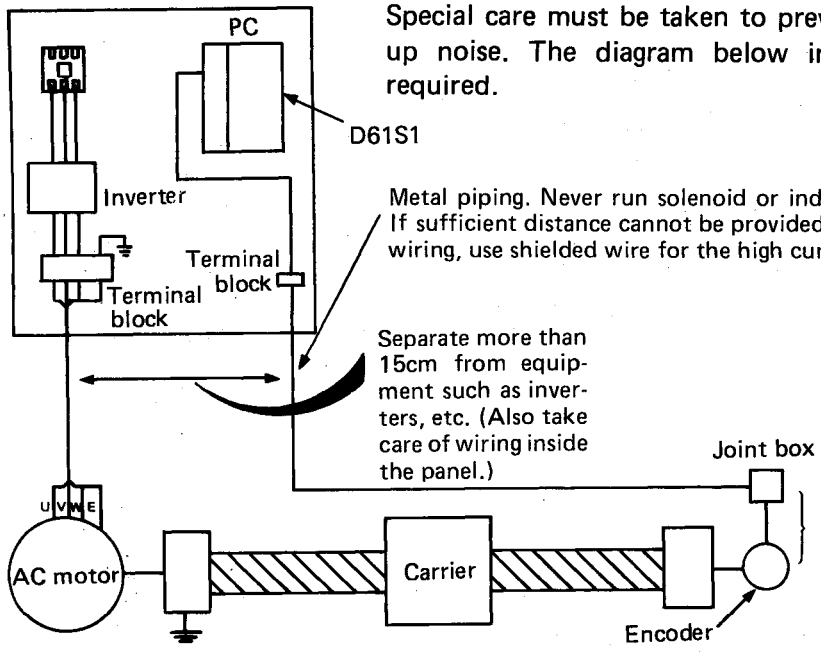
4.1 Wiring

4.1.1 Wiring instructions

When using high speed pulse inputs take precautions against noise in all wiring.

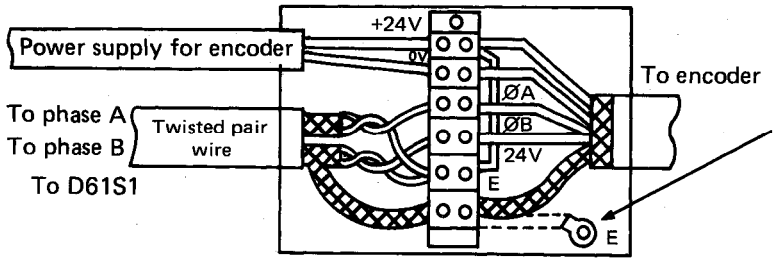
1) Be sure to use shielded twisted pair wires. Also provide Class 3 grounding.
2) Do not run a twisted pair wire in parallel with any power line, I/O line, etc. which may generate noise. It is necessary to run the twisted pair wire separately from the above described lines and over the shortest possible distance.
3) A stabilized power supply is necessary for the pulse generated. For 1-phase input, connect count input signal only to phase A. For 2-phase input, connect count input signal to phase A and phase B.

Special care must be taken to prevent the input wiring from picking up noise. The diagram below indicates the type of precautions required.



Distance between encoder and joint box should be as short as possible. If the distance from the D61S1 to the encoder is too long an excessive voltage drop occurs. Therefore, measure the voltage during operation and check that the voltages are within the rated voltage of the encoder. If the voltage drop is large, increase the size of wiring or use an encoder of 24V DC with less current consumption.

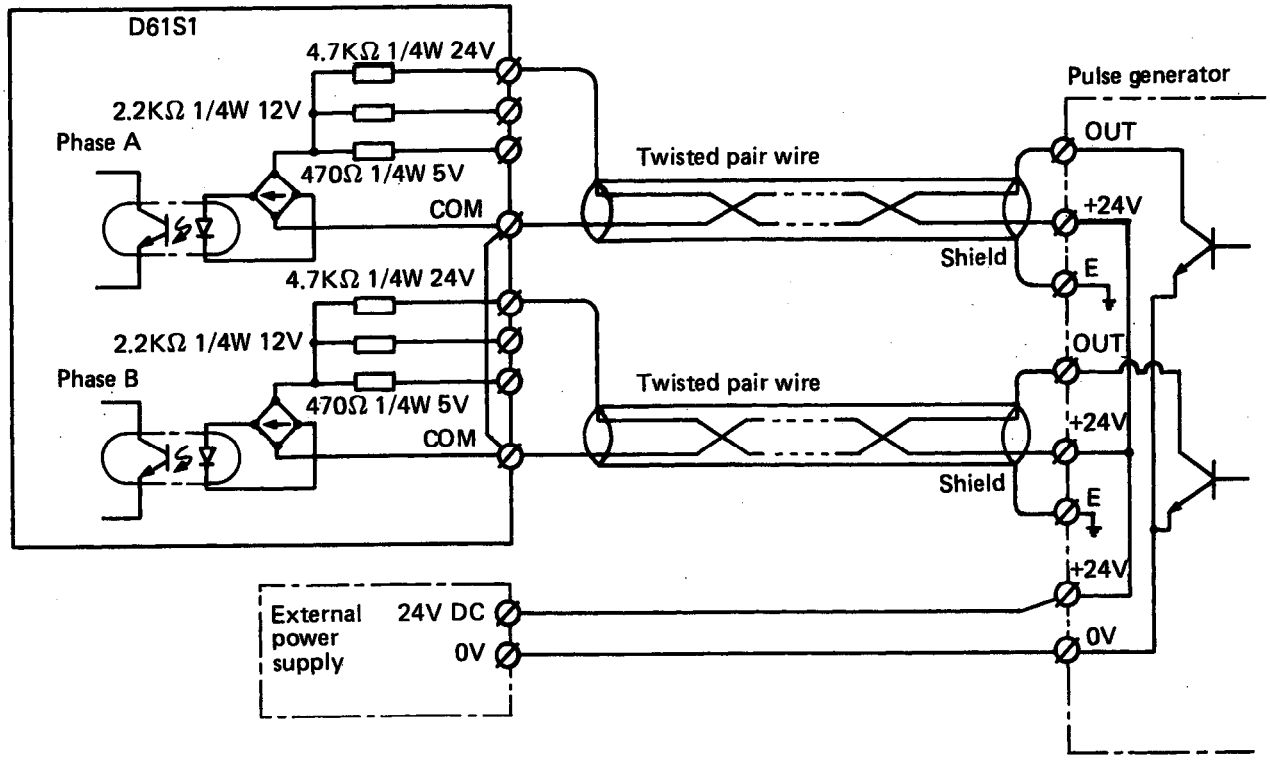
●Ground twisted shield wire on the encoder side (joint box). (This is a connection example for 24V sink load.)



Connect the encoder shield wire to the twisted pair shield wire inside the joint box. If the shield wire of the encoder is not grounded in the encoder, ground it inside the joint box as indicated by dotted line.

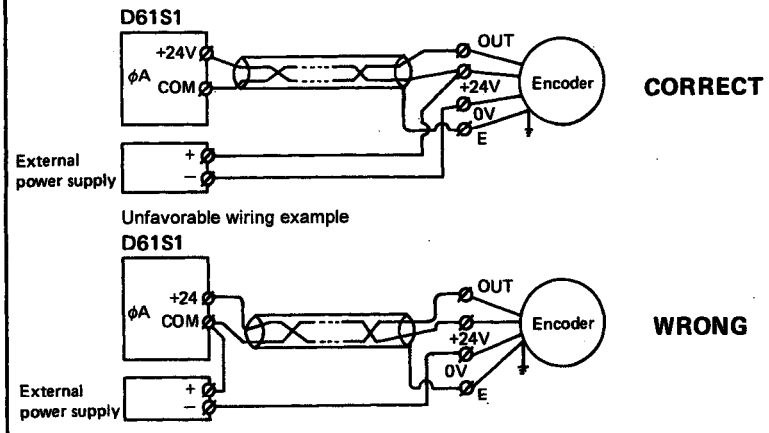
4.1.2 Unit wiring examples

(1) Pulse generator is open collector output (24V DC)



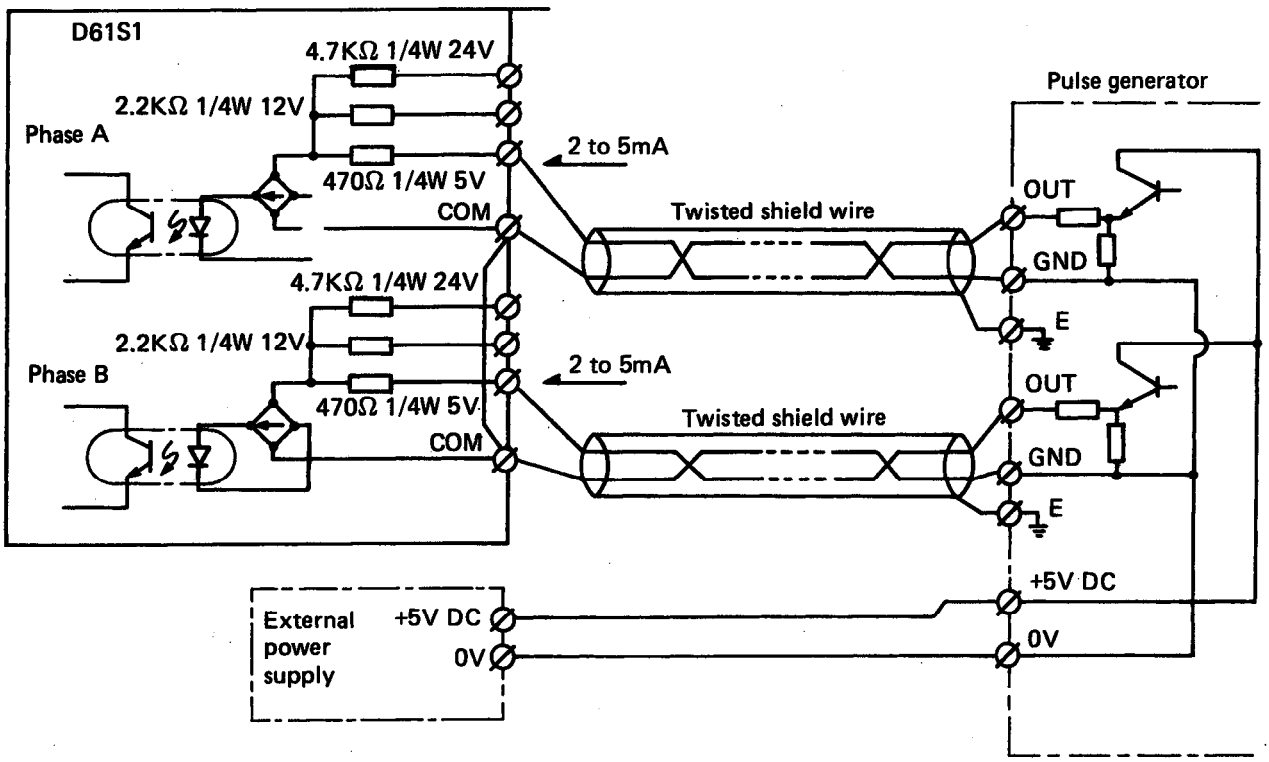
POINT

In order to minimize any interference from noise on the encoder power supply, the encoder signal and supply lines should be wired as follows:

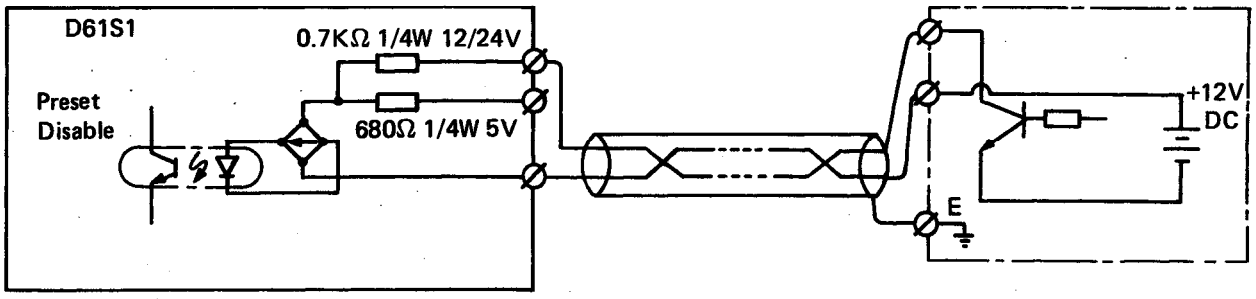


Since the current in the twisted pair wire flow in the same direction, the canceling effect is lost, making the unit subject to electromagnetic induction.

(2) Pulse generator is voltage output type (5V DC)



(3) Connection with input (the same interface for preset and disable)



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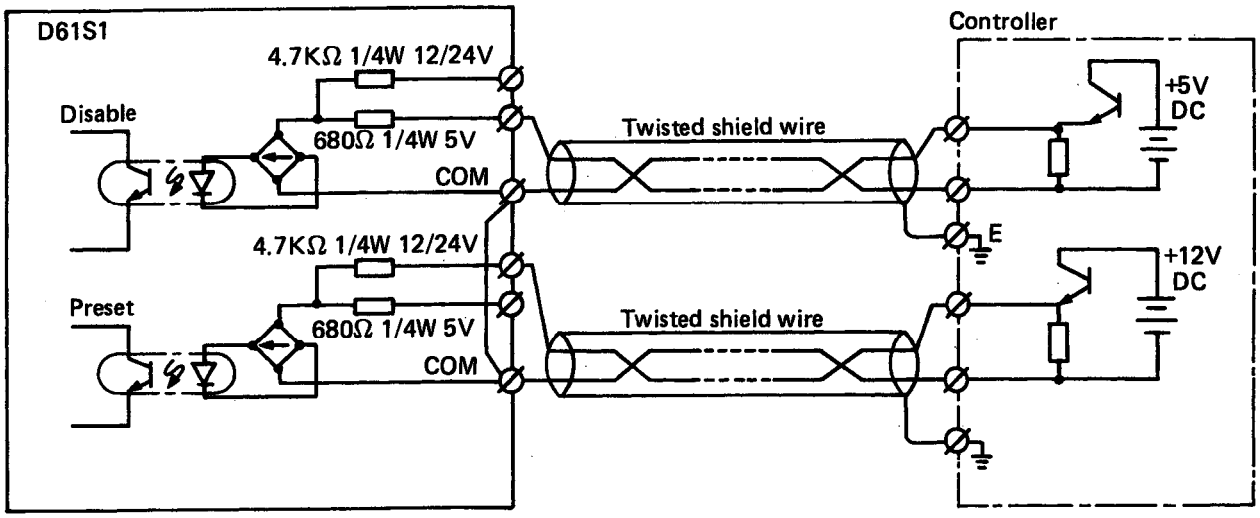
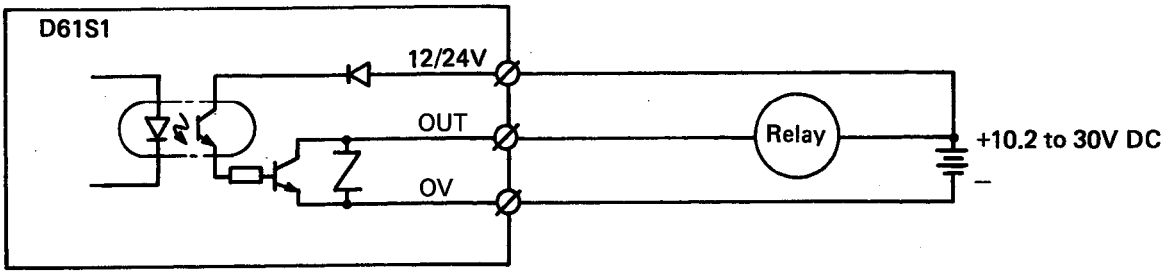
(4) Source load (voltage output type)



(5) Connection with EQU terminal

To use the EQU terminal, the internal photocoupler should be activated. For this purpose, 10.2 to 30V DC external power is necessary. The connection method is as follows:



5. CONCEPT OF THE D61S1 I/O NUMBERS IN A0J2 SYSTEM

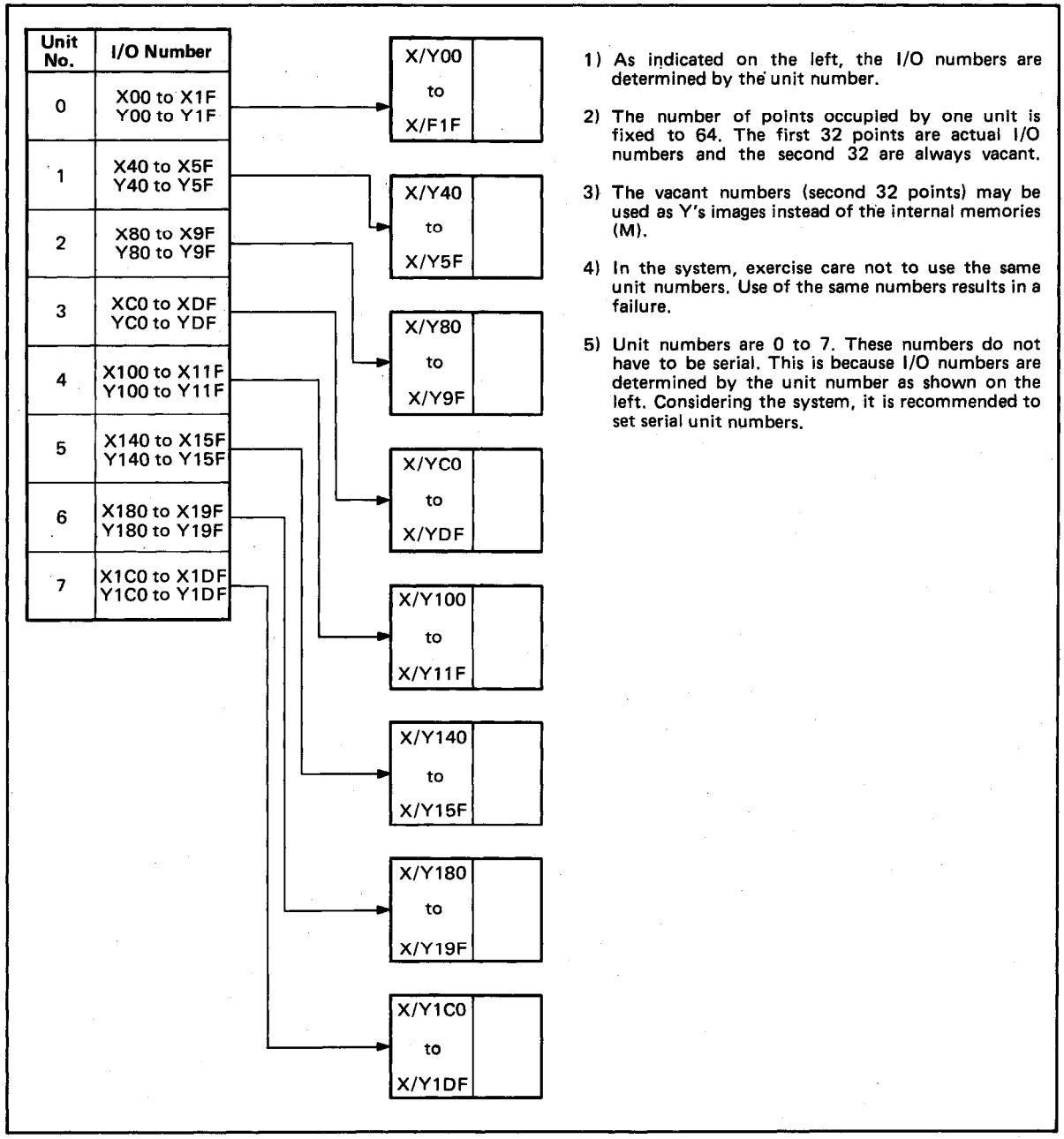
This chapter explains the concept and precautions for the D61S1 I/O numbers in the A0J2 system.

5.1 I/O Number Assignment and Concept

The I/O number assignment is one of the requirements for constructing a system. Wrong assignment will result in failure. Assign the I/O numbers as described below.

(1) X and Y represent inputs and outputs, respectively. I/O numbers are addressed in hexadecimal. (0 to F)

(2) I/O numbers are determined by the unit number set in the D61S1. One unit occupies 64 points.



1) As indicated on the left, the I/O numbers are determined by the unit number.

2) The number of points occupied by one unit is fixed to 64. The first 32 points are actual I/O numbers and the second 32 are always vacant.

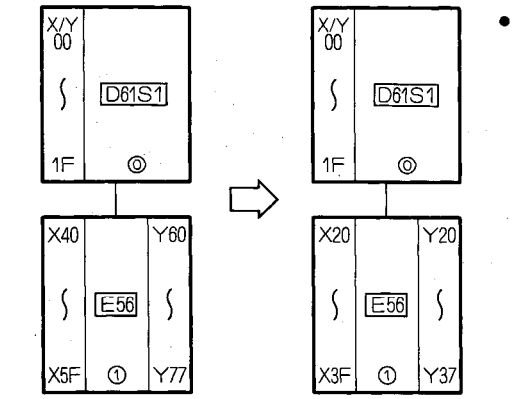
3) The vacant numbers (second 32 points) may be used as Y's images instead of the internal memories (M).

4) In the system, exercise care not to use the same unit numbers. Use of the same numbers results in a failure.

5) Unit numbers are 0 to 7. These numbers do not have to be serial. This is because I/O numbers are determined by the unit number as shown on the left. Considering the system, it is recommended to set serial unit numbers.

5.2 Concept of Parallel I/O Assignment for Use with Remote Station

For the I/O number assignment in a remote station using the A0J2P25/R25, serial and parallel I/O assignments are available. For details, refer to the A0J2 Data Link Unit User's Manual.
This section explains the precaution for parallel I/O assignment.



(Serial I/O assignment) (Parallel I/O assignment)

- As shown on the left, I/O numbers for serial I/O assignment are determined by the unit number (Section 5.1). For parallel I/O assignment, vacant 32 points are shifted to the front and thus the head number of the next unit advances 32 points, e.g. the E56 I/O unit head number advances from X40 to X20 as explained in the left figure.

6. PROGRAMMING

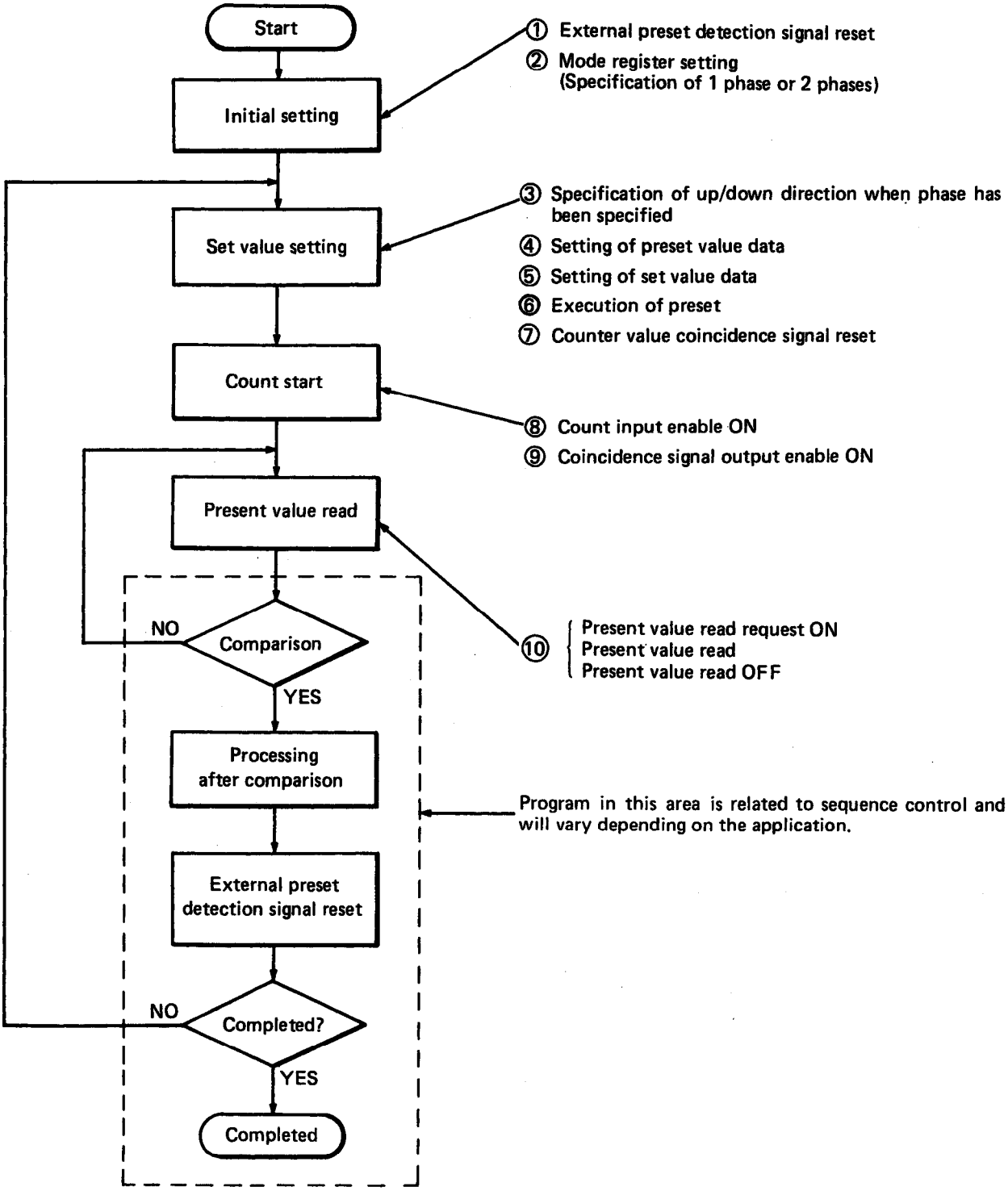
This chapter explains the programming method necessary to use the D61S1.

6.1 General Description of Programming

Program flow for the control of D61S1 is as shown below.

(1) Flow chart and programming procedure when ring counter function is not used (Set the ring counter setting switch to OFF.)

1) Flow chart



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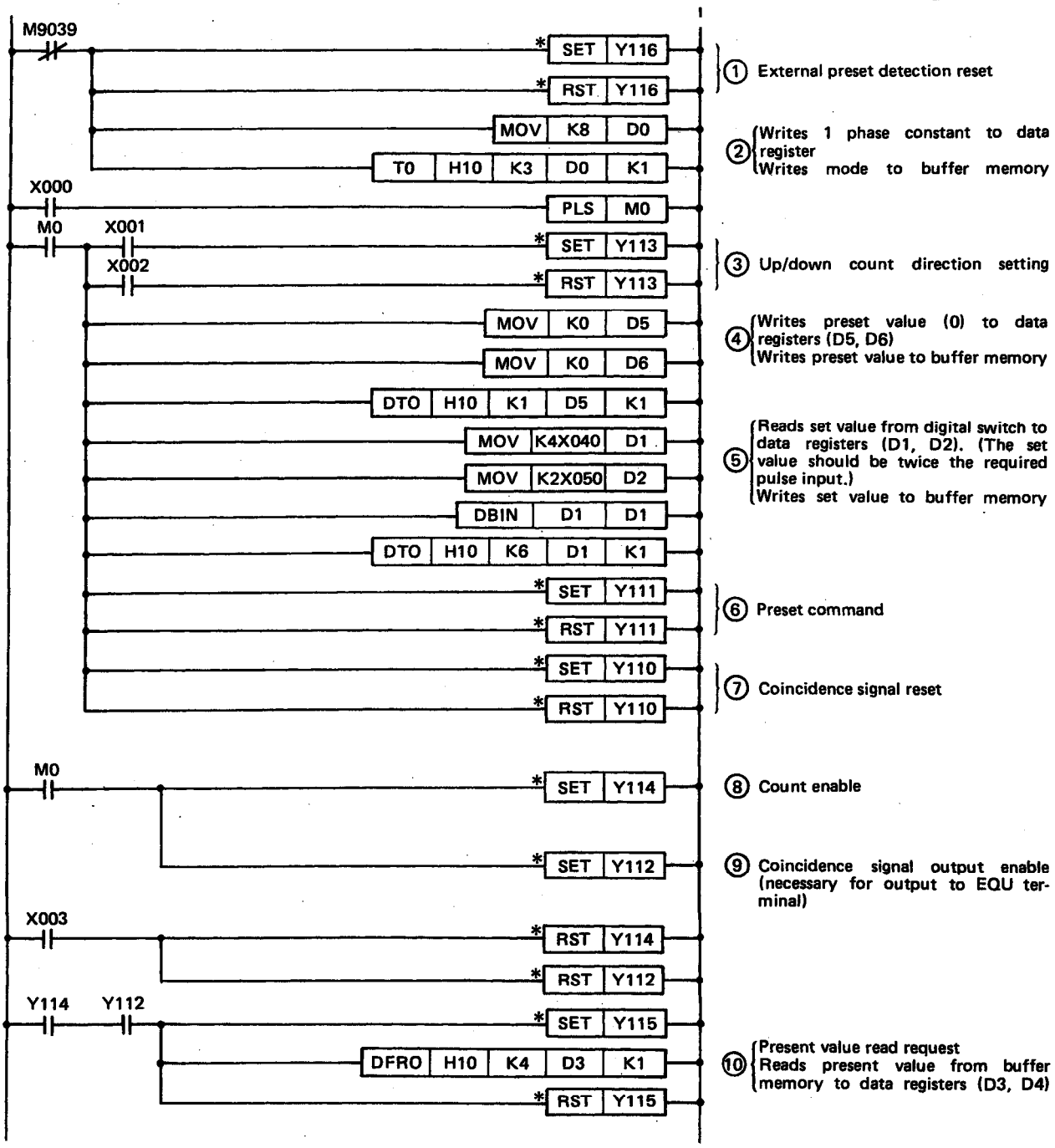
2) Programming procedure

The following example shows a programming procedure relevant to the flow chart in 1).
The D61S1 I/O numbers are assigned to 100 to 11F.
This programming example is in the range ① to ⑩

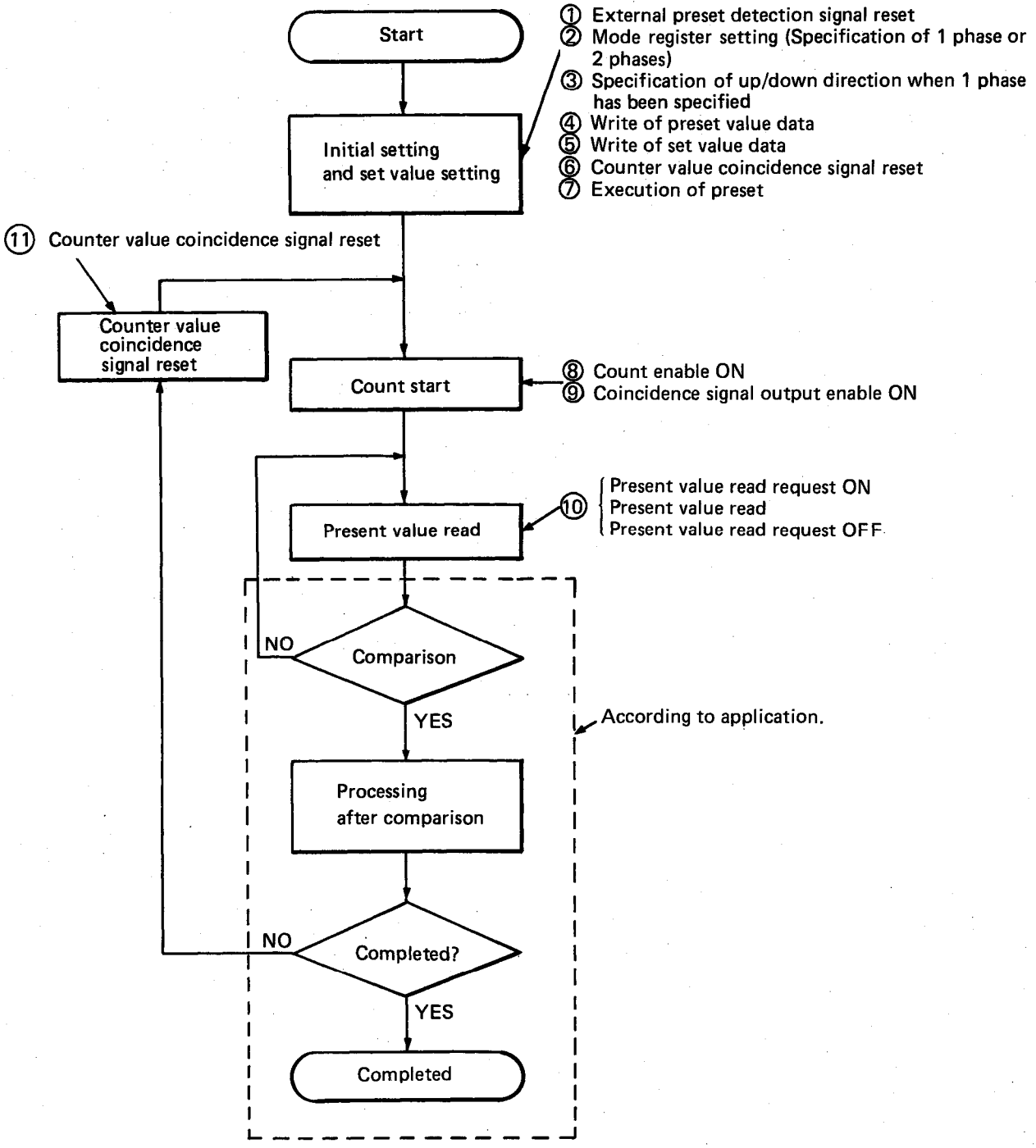


POINT

When the I/O control method of the A0J2HCPU is the refresh mode, the SET/RST instructions cannot be used within the same scan as shown in the above * marked ladder to output pulses to the D61S1. Use the partial refresh (SEG) instruction to output pulses to the D61S1.
Refer to the ACPU Programming Manual for the partial refresh (SEG) instruction.

(2) Flow chart and programming procedure when ring counter function is used (Set the ring counter setting switch to ON.)

1) Flow chart

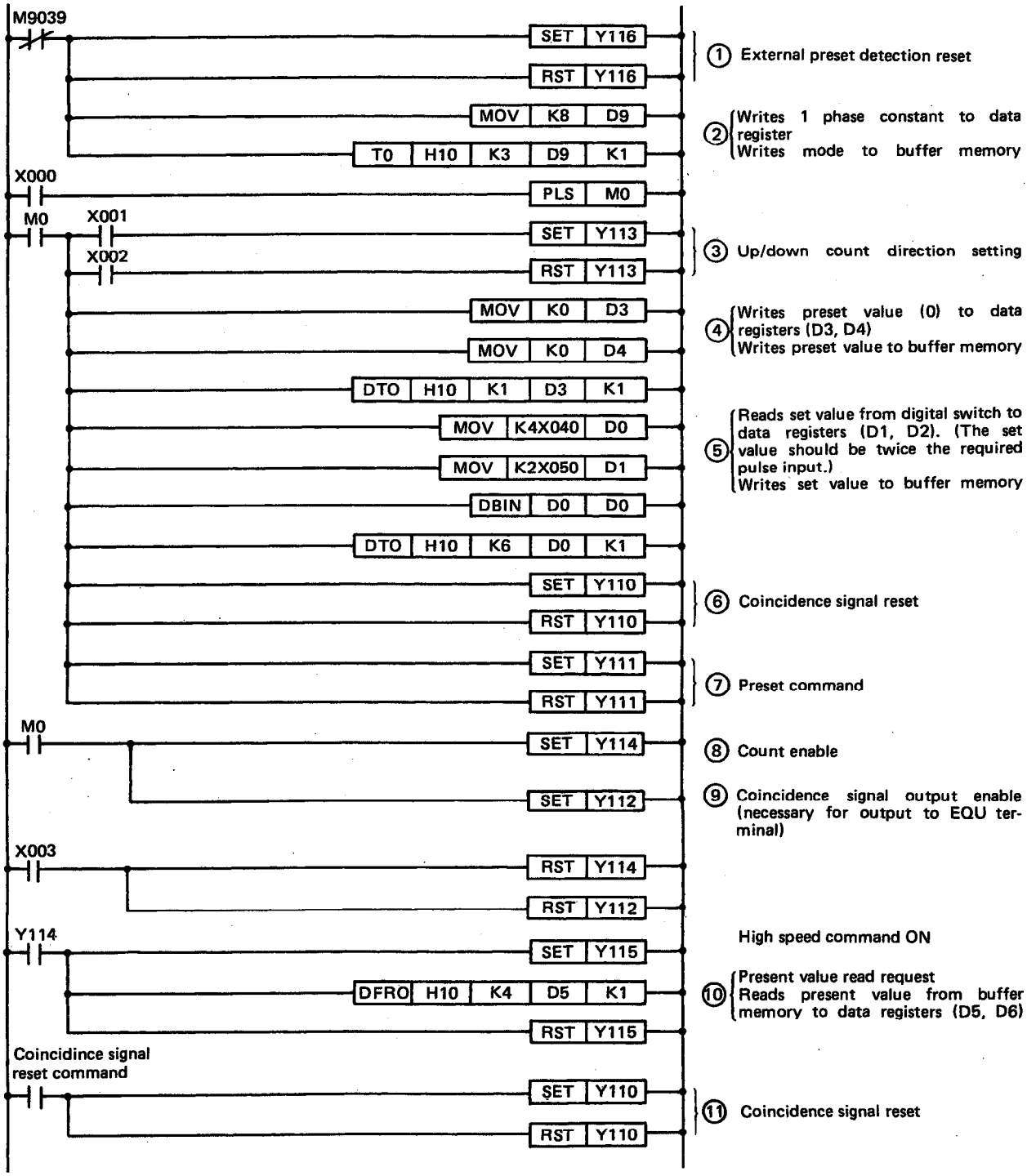


POINT

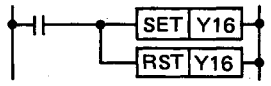
When the ring counter function is used, the next preset cannot be performed if the counter coincidence signal (X01 for CH1, X05 for CH2) remains on. Be sure to reset the counter coincidence signal.

2) Programming procedure

The following example shows a programming procedure relevant to the flow chart in 1).
The D61S1 I/O numbers are assigned to 100 to 11F.
This programming example is in the range ① to ⑪.



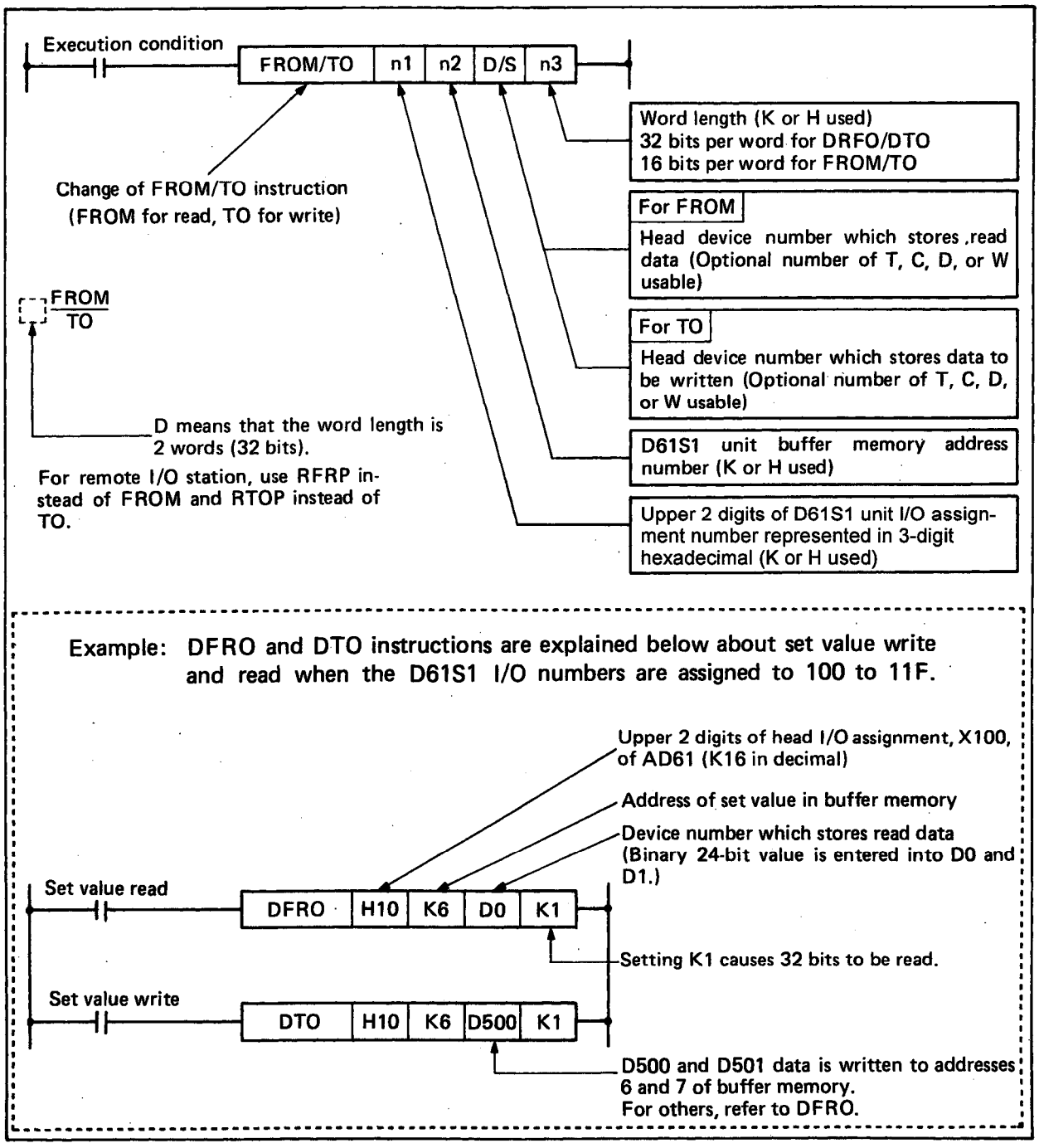
(3) Differences of programming depending on system configurations

System Configuration Using AD61	Instruction or Programming Method Necessary for Use of D61S1	
	Accessing method to buffer memory	D61S1 F/F reset pulse generating method
A0J2CPU independent system. Data link system (A0J2CPUP23/R23 local station).	FROM and TO instructions are used.	SET and RST are used. Example: 
Data link system (remote I/O station). [Remote I/O station (A0J2P25/R25) accessed by master station (A1, A2, A3CPUP21/R21)]	RFRP instruction (equivalent to FROM instruction) RTOP instruction (equivalent to TO instruction) Only one instruction may be executed for 1 special unit within 1 scan.	Since Y output to actual remote I/O station is executed after END of sequence program, pulse is not output by the above method. To output pulse to remote I/O station, create the following program; SET Y16 → END (link refresh) → RST Y16 → END (link refresh).

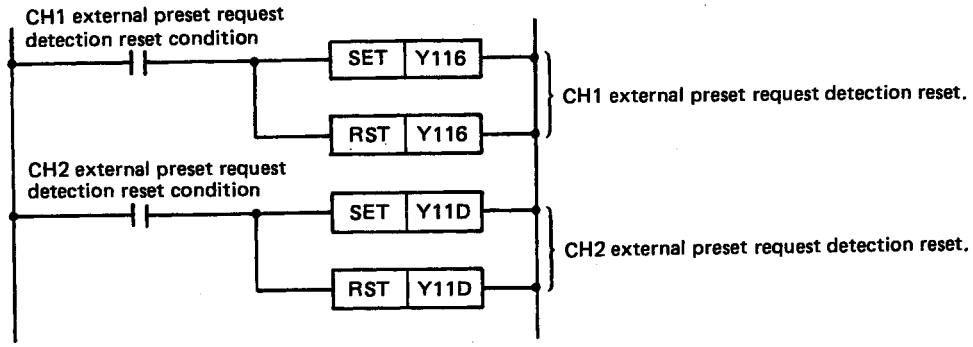
6.2 Programming

This section describes the programming procedure. Explanation will be given in order of programming flow chart in Section 6.1

To use any special function unit, utilize FROM and TO instructions. These instructions will be described below. For details, refer to the A0J2CPU and A1, A2, A3CPU Programming Manuals.

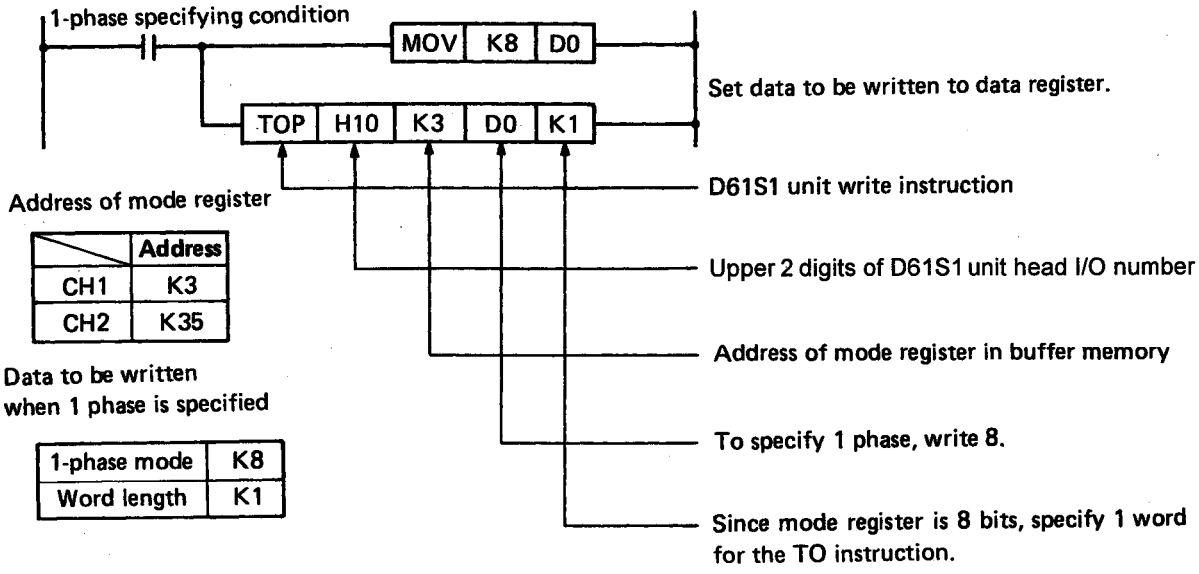


(1) External preset detection reset



- To perform preset from outside, it is necessary to perform reset of external preset each time.
- Since the preset operation occurs on the pulse leading edge, further, preset by external input or preset by sequence program cannot be performed until the external preset flip flop has been reset.
- The external preset flip flop can be reset while the external preset input is on.
- It is not necessary to execute this signal if the external preset terminal is not used.

(2) Setting of mode register (1-phase specification)



Address of mode register

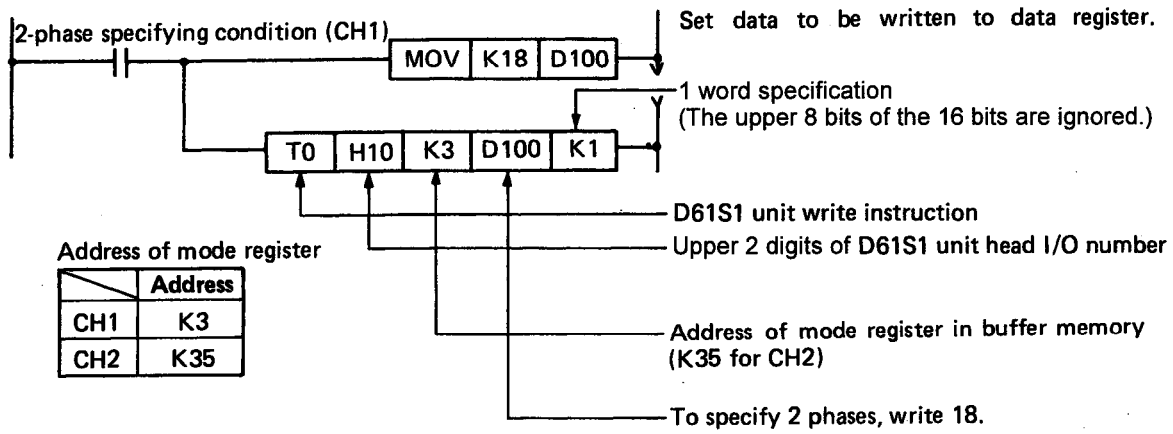
	Address
CH1	K3
CH2	K35

Data to be written when 1 phase is specified

1-phase mode	K8
Word length	K1

- **Since the value of the mode register is 0 when the power is switched on or the CPU is reset, be sure to write 8 when using the unit in 1 phase.**
- For the specification of up or down count, refer to Section (4).

(3) Setting of mode register (2-phase specification)



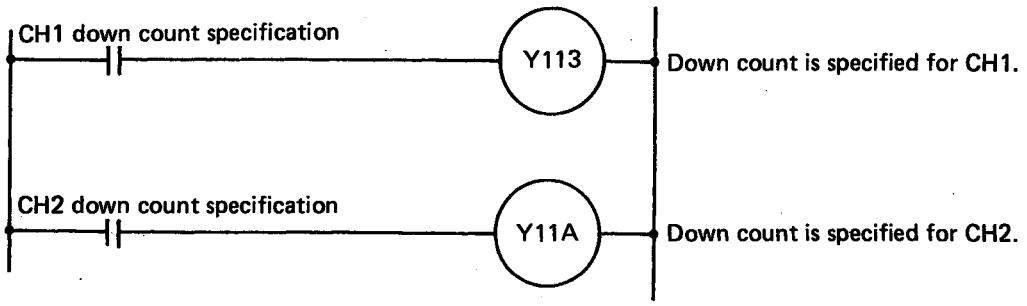
Address of mode register

	Address
CH1	K3
CH2	K35

Data to be written when 2 phases have been specified (in decimal)

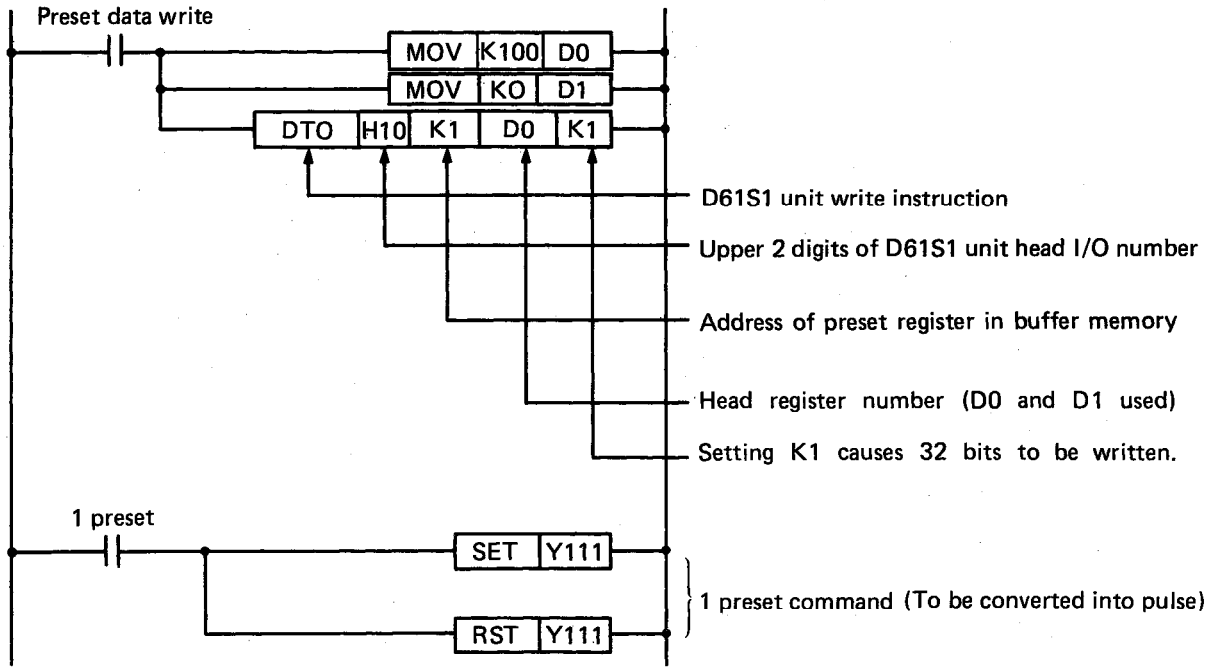
2-phase mode	K18
Word length	K1

(4) Setting of up/down count when 1-phase has been specified.



- When Y113 or Y11A is off, up count is made.
- When the power is turned on or the CPU is reset, both Y113 and Y11A are off.

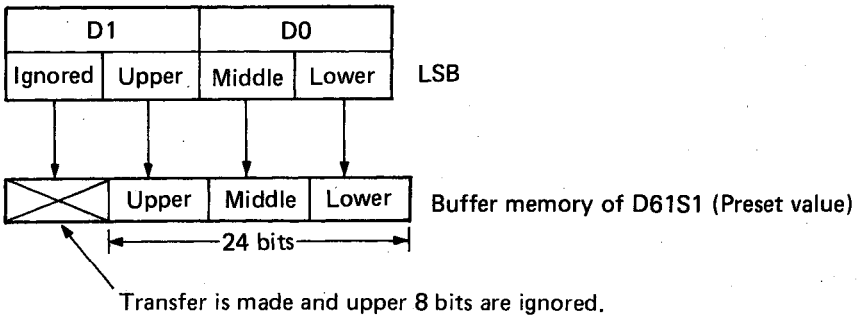
(5) Setting of preset value data (to set preset value to 100)



1) Address of preset value

	Address
CH1	K1
CH2	K33
Word length	K1

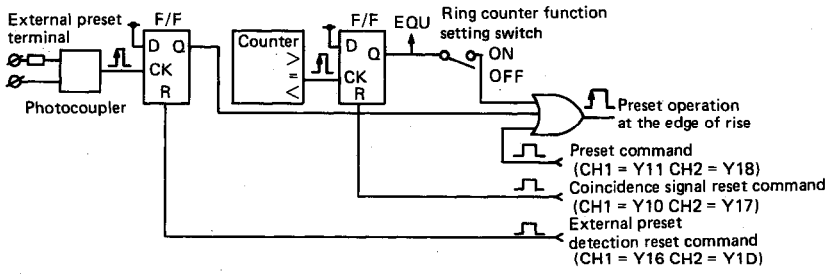
2) Write operation



3) When the preset command signal turns on, the preset value is set as the initial value for the counter on the signal's leading edge.
   - ○ If the external preset request detection signal remains on, preset cannot be preformed even when the above instructions are executed. Before turning on preset, it is necessary to execute external preset detection signal reset.
   - ○ Preset can be executed at any positions after the preset value is written.

POINT

A block diagram related to the preset operation of the D61S1 is shown below.

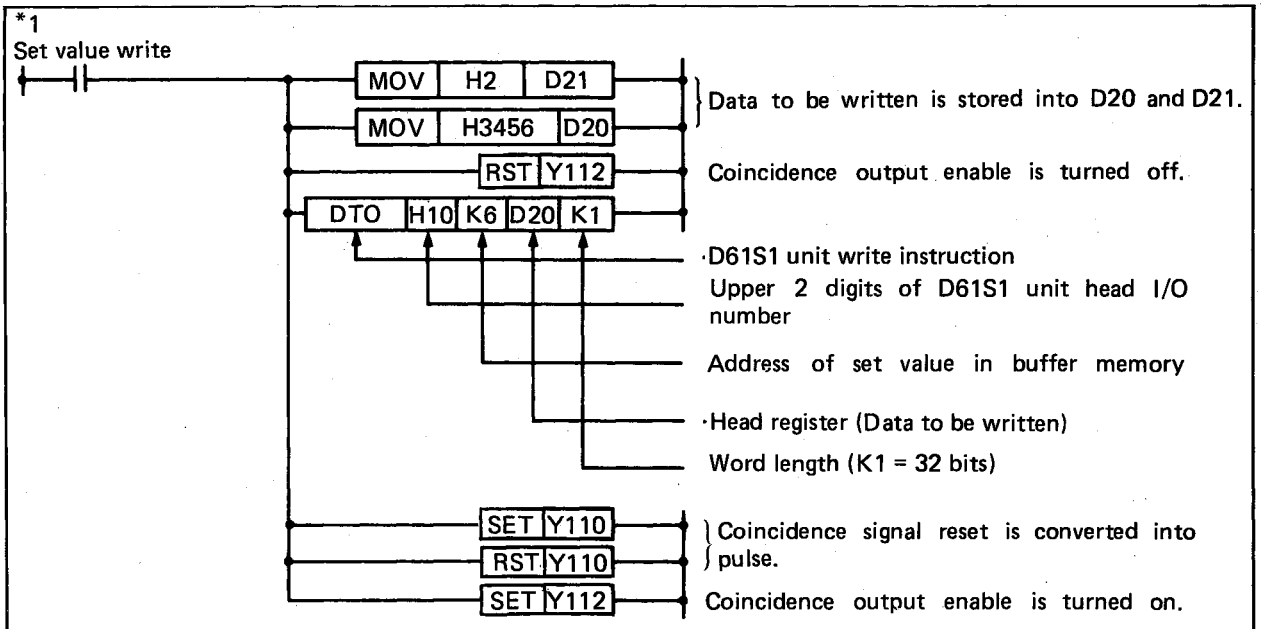


Three signals are available for preset operation.

1. **Preset by program**
2. **Input from external preset terminal**
3. **Counter coincidence when ring counter is on**

Preset operation uses logical add (OR) of these three signals. Upon rise of this signal from off to on, preset operation is performed. If one of the signals remains on, preset operation is not performed because, if another preset signal is turned from off to on, the output of logical add remains on. When ring counter function has been selected, counter value coincidence signal (preset signal) and external preset signal are latched by flip flop. Therefore, it is necessary to provide a reset signal to each of them.

(6) Setting of set value data



Set value address and signal

	Address	Coincidence output enable	Coincidence signal reset
CH1	K6	Y112	Y110
CH2	K38	Y119	Y117
Word length	K1		

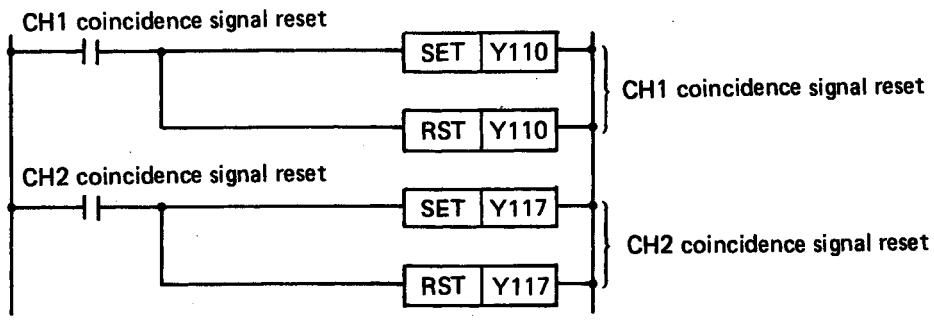
○Convert the instruction marked *1 into pulse.

○When external EQU terminal is not used, RST Y112 and SET Y112 are not required.

○ When the set value data is written to the buffer memory, the counter value coincidence signal may turn on. For this reason, turn off the coincidence output enable before the set value is written, reset the coincidence signal and finally re-enable the coincidence output.

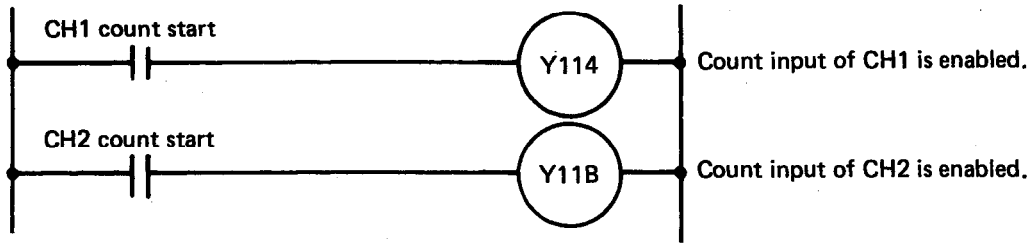
IB (NA) 66094-A

(7) To reset coincidence signal



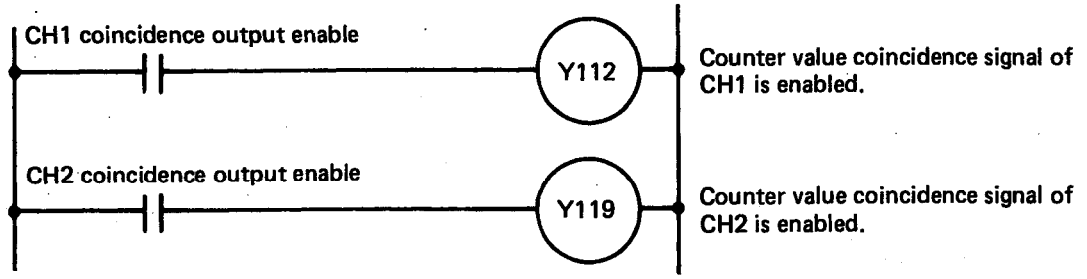
When Y110 is on, the coincidence signal (X101) of channel 1 is not output.
Be sure to convert it into a pulse with SET or RST.

(8) To enable count input



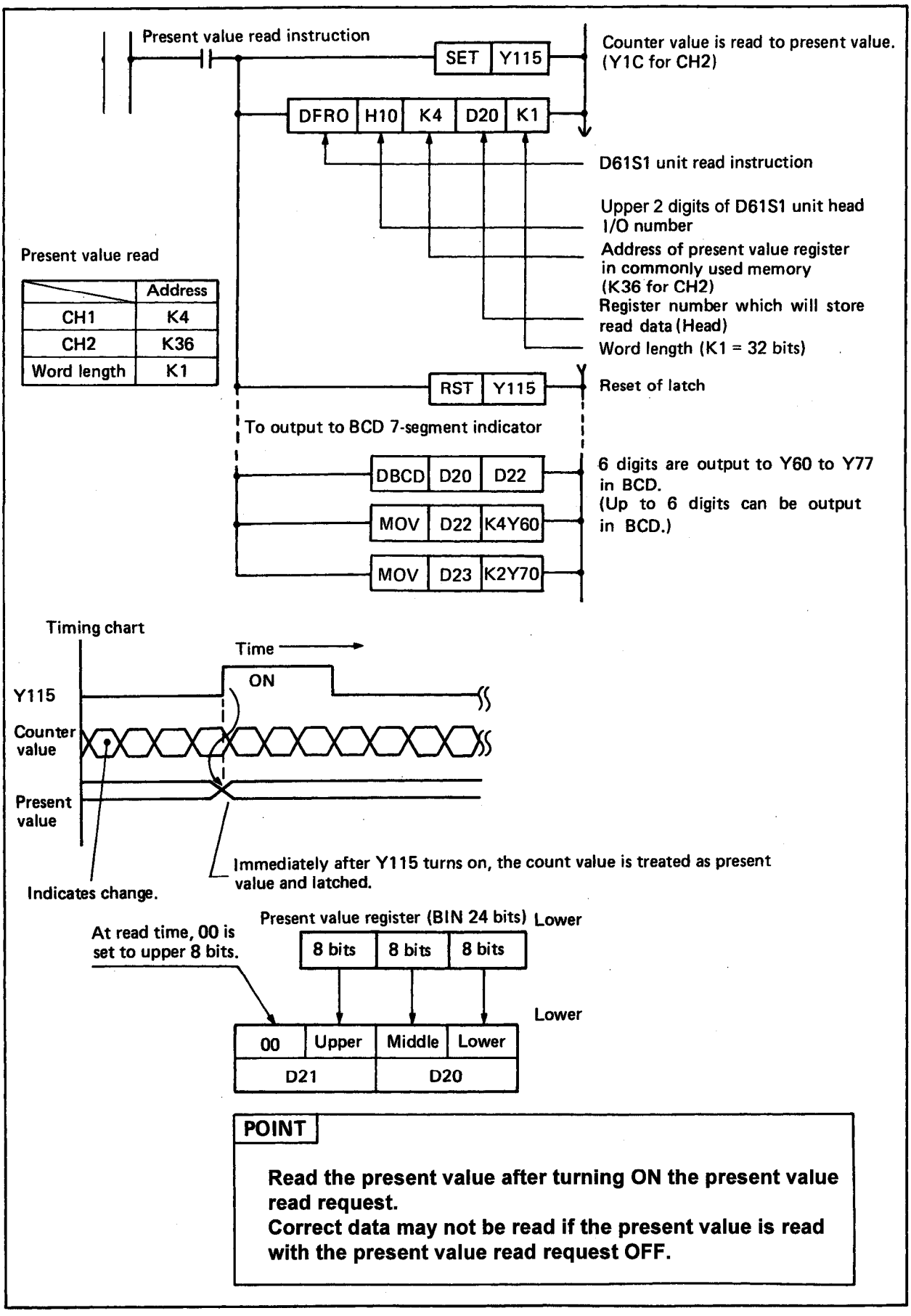
To count signals from the count input terminal block, this signal should be on and the disable input of external terminal block should be off.

(9) To enable coincidence signal output



If a counter value is equal to a set value after this signal is turned on, the counter value coincidence signal is output to the EQU terminal. At the same time, "EQU" LED on the indicator at the top of D61S1 is lit.

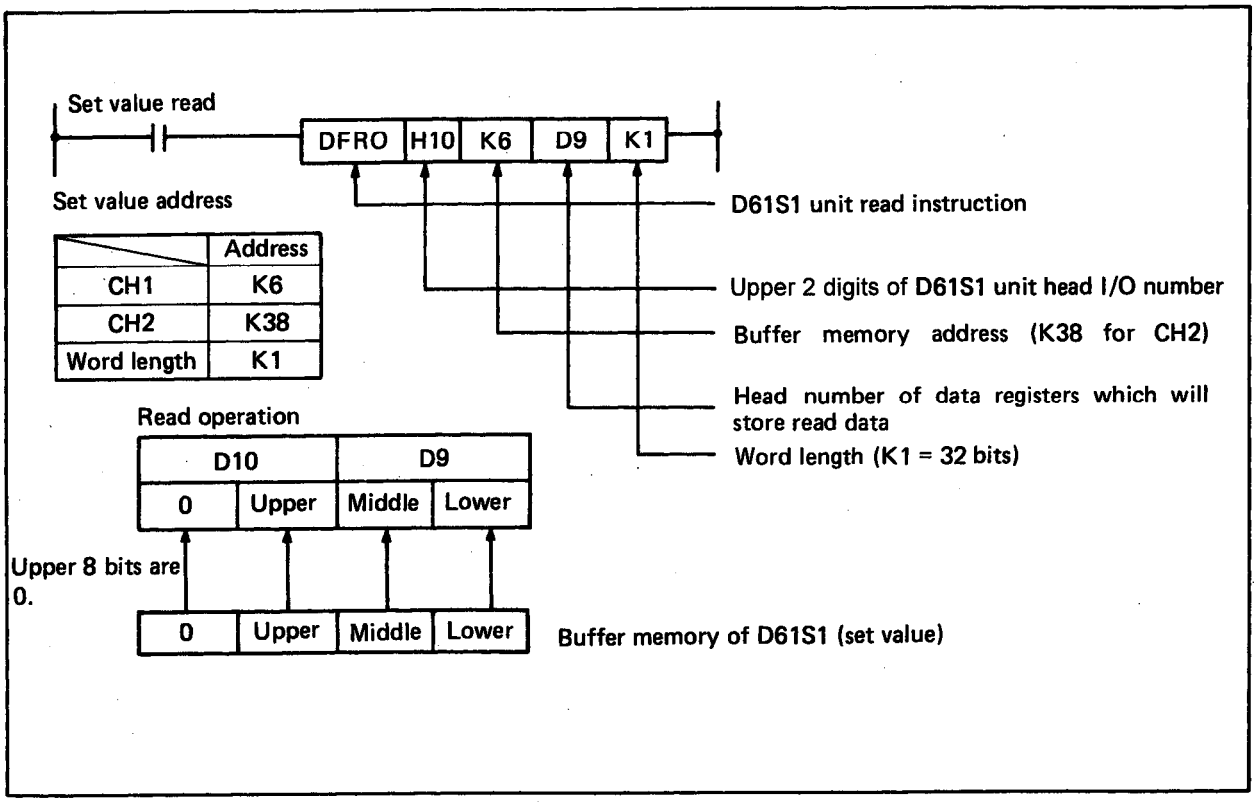
(10) Present value read



POINT

Read the present value after turning ON the present value read request.
Correct data may not be read if the present value is read with the present value read request OFF.

(11) Set value read



6.3 Programming for Using the D61S1 in Remote I/O Station

This section explains programming for the master station (ACPU) when the D61S1 is loaded in a remote I/O station.

6.3.1 Programming instructions

The ACPU I/O control method is a direct method. However, data communications to and from the remote I/O station are made in the batch refresh method after the END (FEND) instruction is executed. Hence, when the D61S1 is loaded in the remote I/O station, use care for the following points. For detailed data link specifications, refer to the Data Link Unit User's Manual.

(1) Since control data between the master station CPU and remote I/O station D61S1 is controlled via the link unit, a time difference (response delay) occurs. Caution should be exercised for control timing.

(2) For data communications with the D61S1 in the remote I/O station, use the following instructions:

Data write from the master station to the D61S1:
RTOP instruction
Data read from the D61S1 to the master station:
RFRP instruction

Data communications between the master station CPU and D61S1 are made using the link registers (W). Therefore, create a processing program, as required, which transfers the link register contents to the other device after execution of the RFRP instruction or transfers data to be transferred to the link registers before execution of the RTOP instruction.

(3) The RTOP and RFRP instructions access from the master station to the remote I/O station. However, since these instructions cannot be executed during the same scan, always use interlock signals. For the interlocking procedure, refer to Fig. 6.1. For the programming procedure, refer to Section 6.3.2.

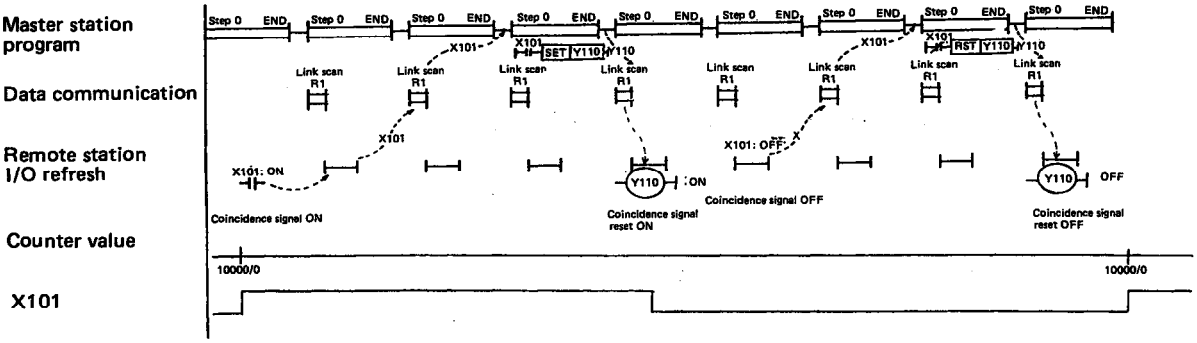
(4) Control signal to D61S1

- Because of the relation between the master station scan time and link scan time, Y□□ may not be output to the remote I/O station using PLS Y□□.

- Since data communications between the master station and remote I/O station are made in the batch refresh method after execution of the END (FEND) instruction, pulse output which executes the RST instruction after the SET instruction execution cannot be used.

POINT

Several scans are required until all handshake signals are completed between the D61S1 and master station CPU. Caution should be exercised in the following example in which the counter coincidence signal (X01) is reset using the coincidence signal reset command (Y10). In this case, the D61S1 is assigned to a slot corresponding to the head I/O number X/Y100 and the set value is 10000. (The head I/O numbers of the master and remote I/O stations are X/Y100.)



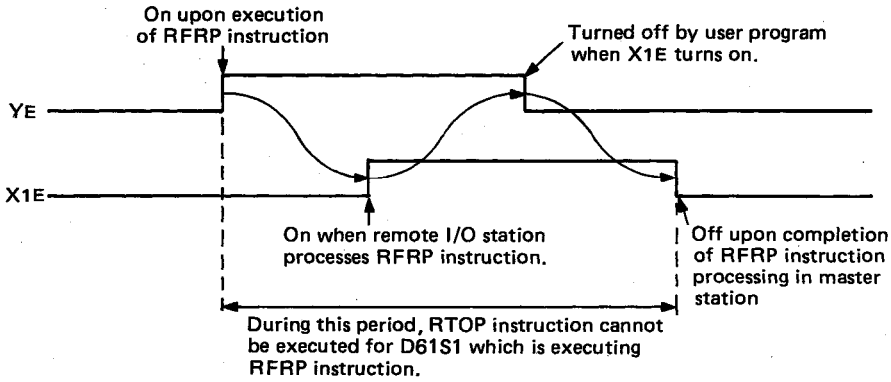
In the above example, the counting time from 0 to the set value (10000) by the counter is longer than the handshake time between the D61S1 and PC CPU. Therefore, the D61S1 operates properly.

If the counting time is shorter than the handshake time (the set value is smaller than 10000 or the counting pulse frequency is greater), the D61S1 may misoperate or count a value greater than the set value.

In such a case, the D61S1 cannot be used in the remote I/O station. Therefore, load the D61S1 in the local station or use the COM instruction in the program. (For the COM instruction, refer to the Data Link Unit User's Manual.)

⟨Signal Direction⟩ Master Station CPU to D61S1		⟨Signal Direction⟩ D61S1 to Master Station CPU	
Device No.	Signal	Device No.	Signal
Y0 to YD	Unusable.	X10 to X1D	Unusable.
YE	On at RFRP instruction execution. To be reset by user program after checking that X1E is on.	X1E	On while the remote I/O station is processing the RFRP instruction.
YF	On at RTOP instruction execution. To be reset by user program after checking that X1F is on.	X1F	On while the remote I/O station is processing the RTOP instruction.

During RFRP instruction execution



During RTOP instruction execution

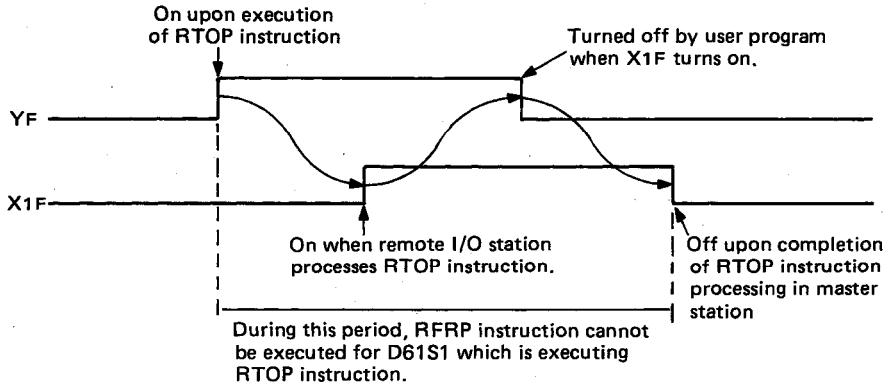
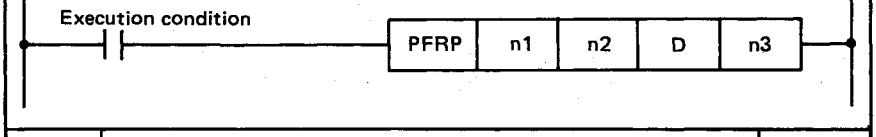


Fig. 6.1 Interlock Signals

6.3.2 Basic programs for read and write

(1) Read from remote I/O station D61S1

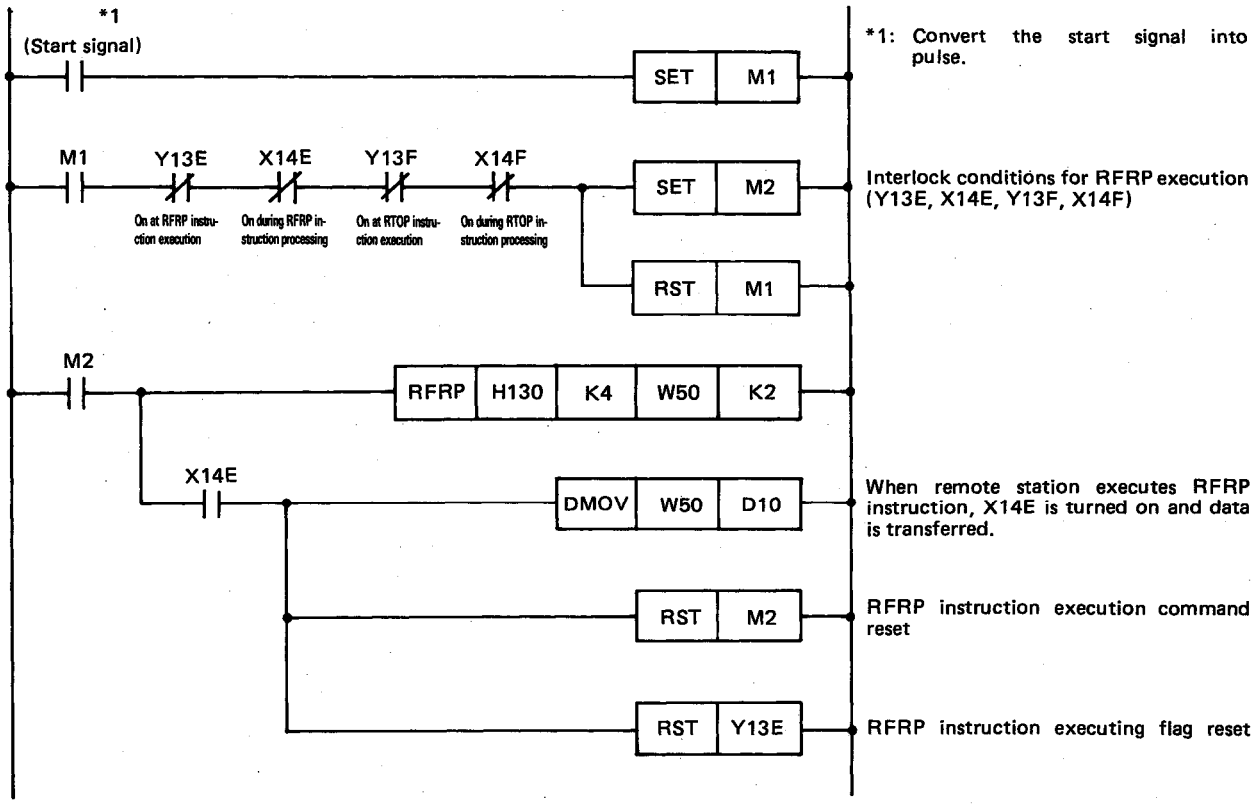
Format



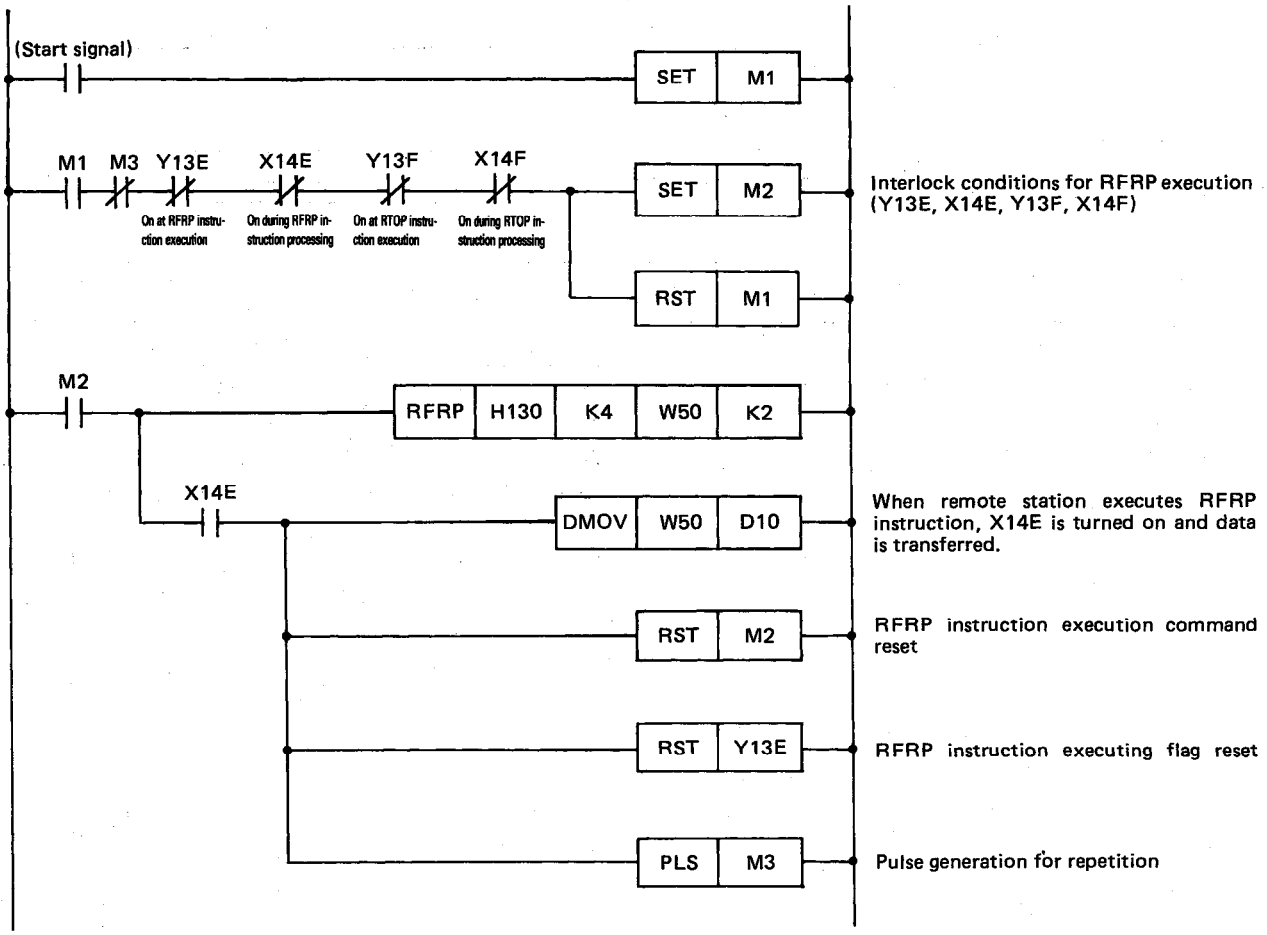
Symbol	Description	Available Device
n1	Head 3 digits of the D61S1 I/O number assigned from master station	K, H
n2	Head address of D61S1 buffer memory which stores data to be read	K, H
D	Head number of link registers which will store read data	W
n3	Number of data to be read	K, H

Example: To read two words from the buffer memory addresses 4 and 5 (present value) in the remote I/O station D61S1, corresponding to X, Y130 to 14F assigned from the master station, to W50 and W51.

To execute only once by turning on the start signal



To keep executing while the start signal is on

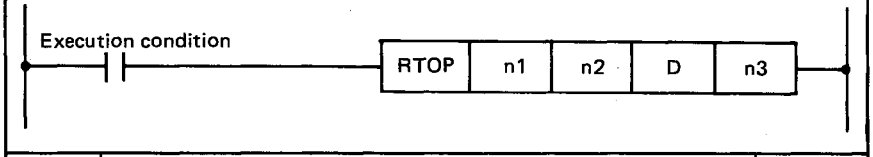


POINT

The head I/O number specified at n1 is of three digits for the RFRP and RTOP instructions.

(2) Write to remote I/O station D61S1

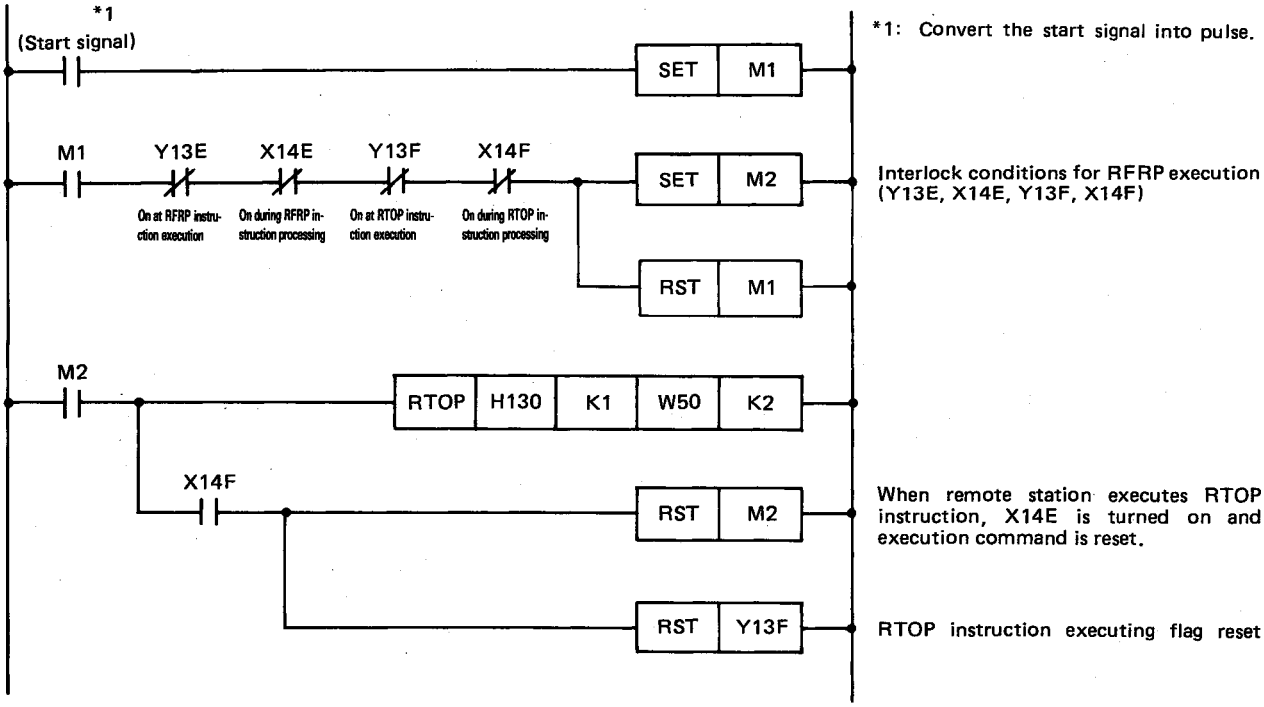
Format



Symbol	Description	Available Device
n1	Head 3 digits of the D61S1 I/O number assigned from master station	K, H
n2	Head address of D61S1 buffer memory to which data will be written	K, H
D	Head number of link registers which store data to be written	W
n3	Number of data to be written	K, H

Example: To write two words from link registers, beginning with W50, to the buffer memory addresses 1 and 0 (preset value) in the remote I/O station D61S1 corresponding to X, Y130 to 14F assigned from the master station.

To execute only once by turning on the start signal



POINT

The head I/O number specified at n1 is of three digits for the RFRP and RTOP instructions.

6.3.3 Program example

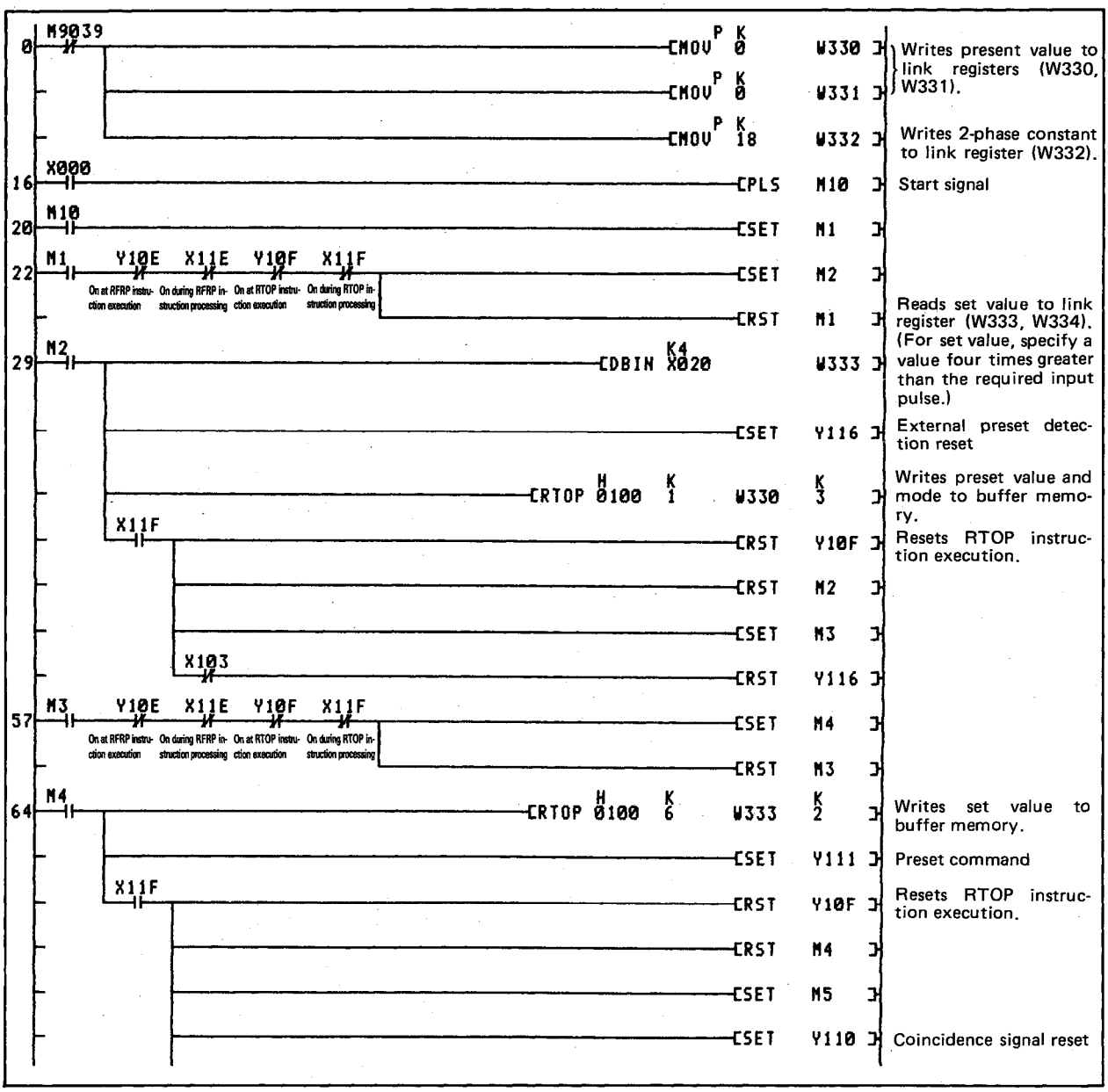
The following program monitors a present value with the D61S1 loaded in the remote I/O station. Conditions are as follows:

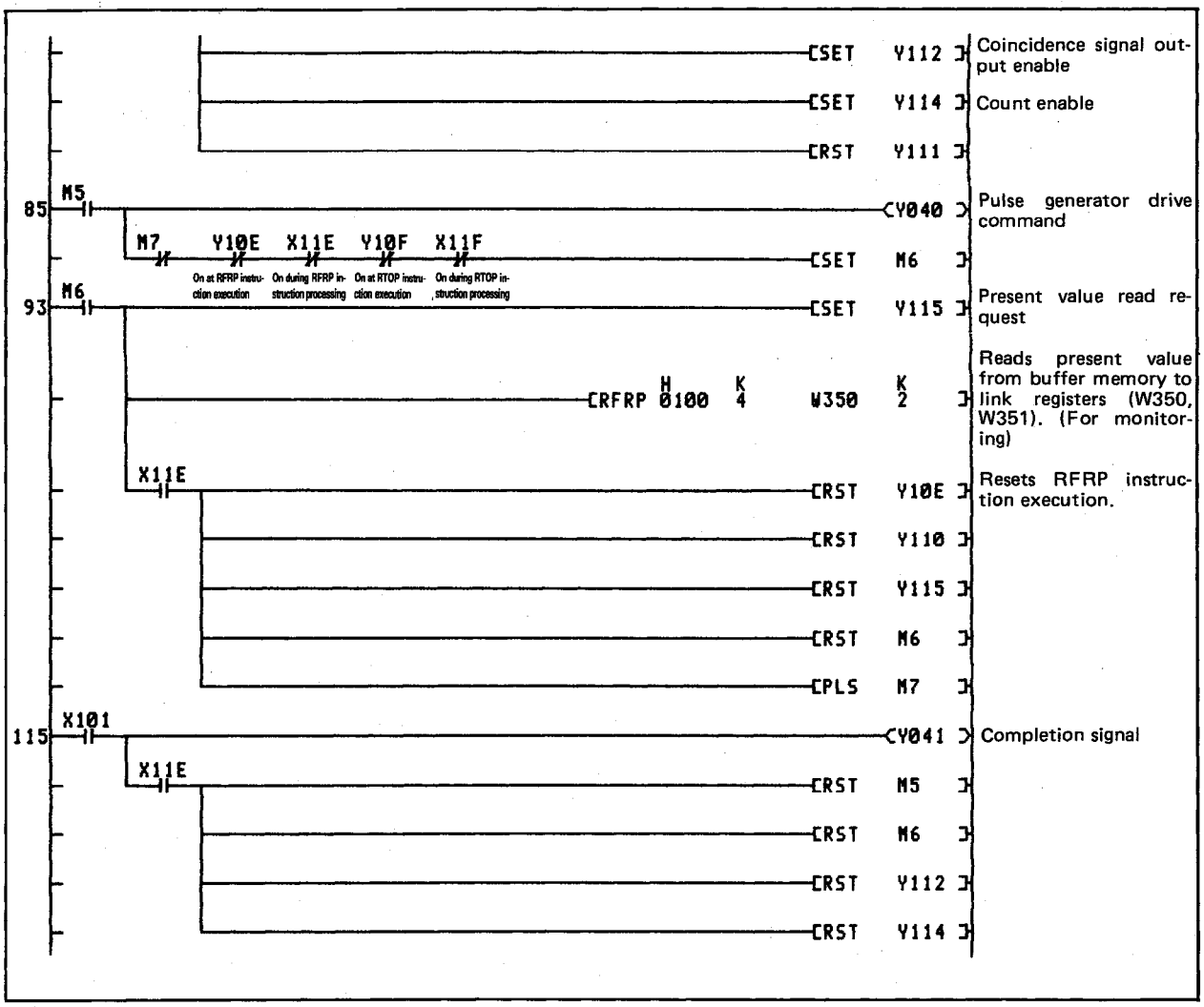
(1) The D61S1 has been assigned to X/Y100 to 11F from the master station.

(2) Link registers used are W320 to 33F (32 points) for the RTOP instruction and W350 to W36F (32 points) for the RFRP instruction.

(3) Device assignment

W330, W331: preset value, W332: mode, W333, W334: set value, W350, W351: present value, X0: start command, Y40: pulse generator drive command, Y41: completion signal




SET Y112
Coincidence signal output enable
SET Y114
Count enable
RST Y111
85 M5
Y040
Pulse generator drive command
M7 Y10E X11E Y10F X11F
On at RFRP instruction execution
On during RFRP instruction processing
On at RTOP instruction execution
On during RTOP instruction processing
SET M6
93 M6
SET Y115
Present value read request
RFRP H 0100 K 4 W350 K 2
Reads present value from buffer memory to link registers (W350, W351). (For monitoring)
X11E
RST Y10E
Resets RFRP instruction execution.
RST Y110
RST Y115
RST M6
PLS M7
115 X101
Y041
Completion signal
X11E
RST M5
RST M6
RST Y112
RST Y114

7. TEST OPERATION

7.1 Pre-test Checks

IMPORTANT

Before switching on the encoder power supply, check that the correct terminals have been used. Application of 24V to 5V terminals will damage the unit.

Before turning on the power, check the following:

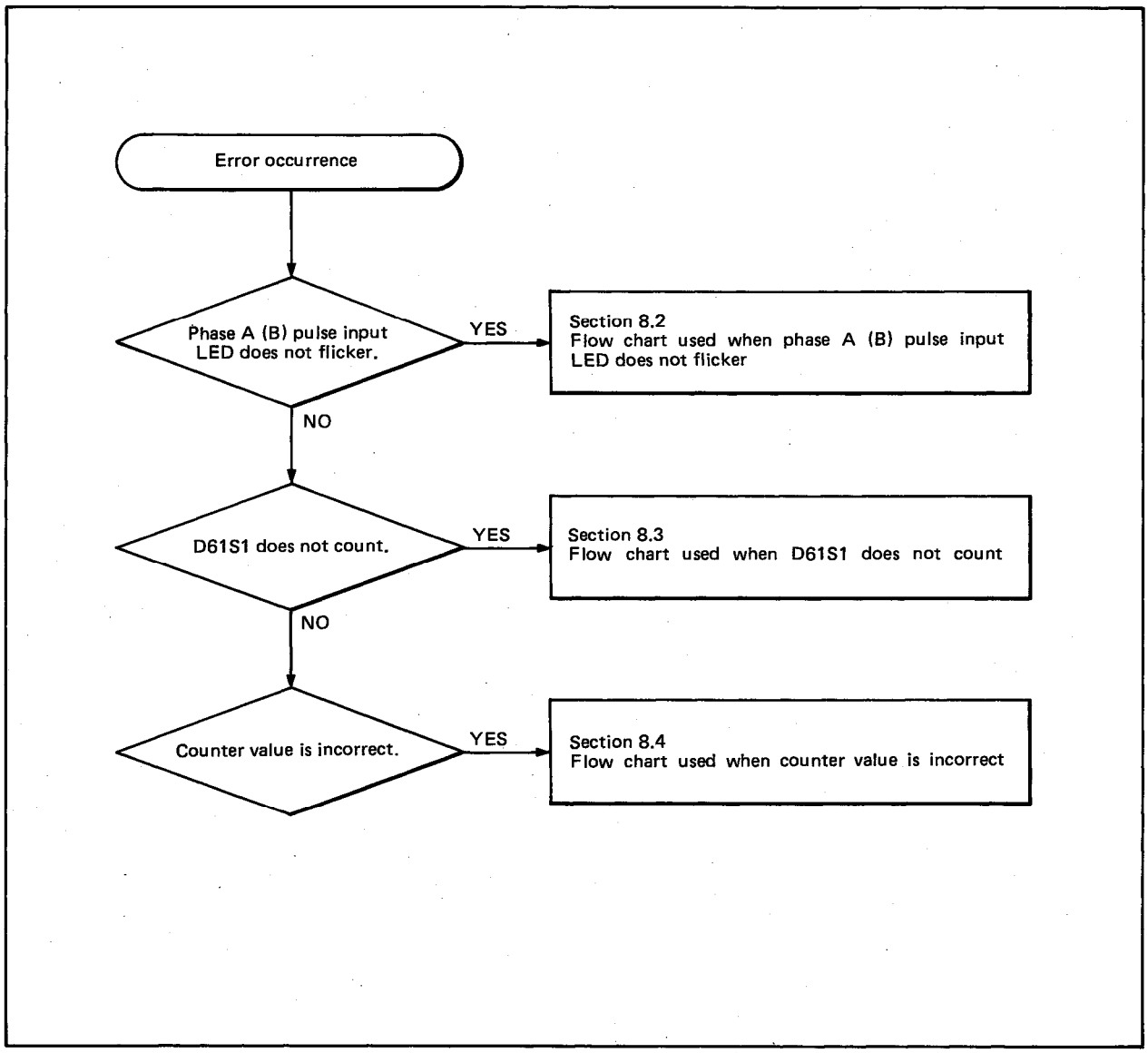
1. Ring counter setting switch.
2. Check that the D61S1 cable is properly connected.
3. Check terminal wiring.
4. Check the voltage of the external power supply.

After the above checks, turn on the power and operate the pulse generator. Check the relevant phase indicator LED.

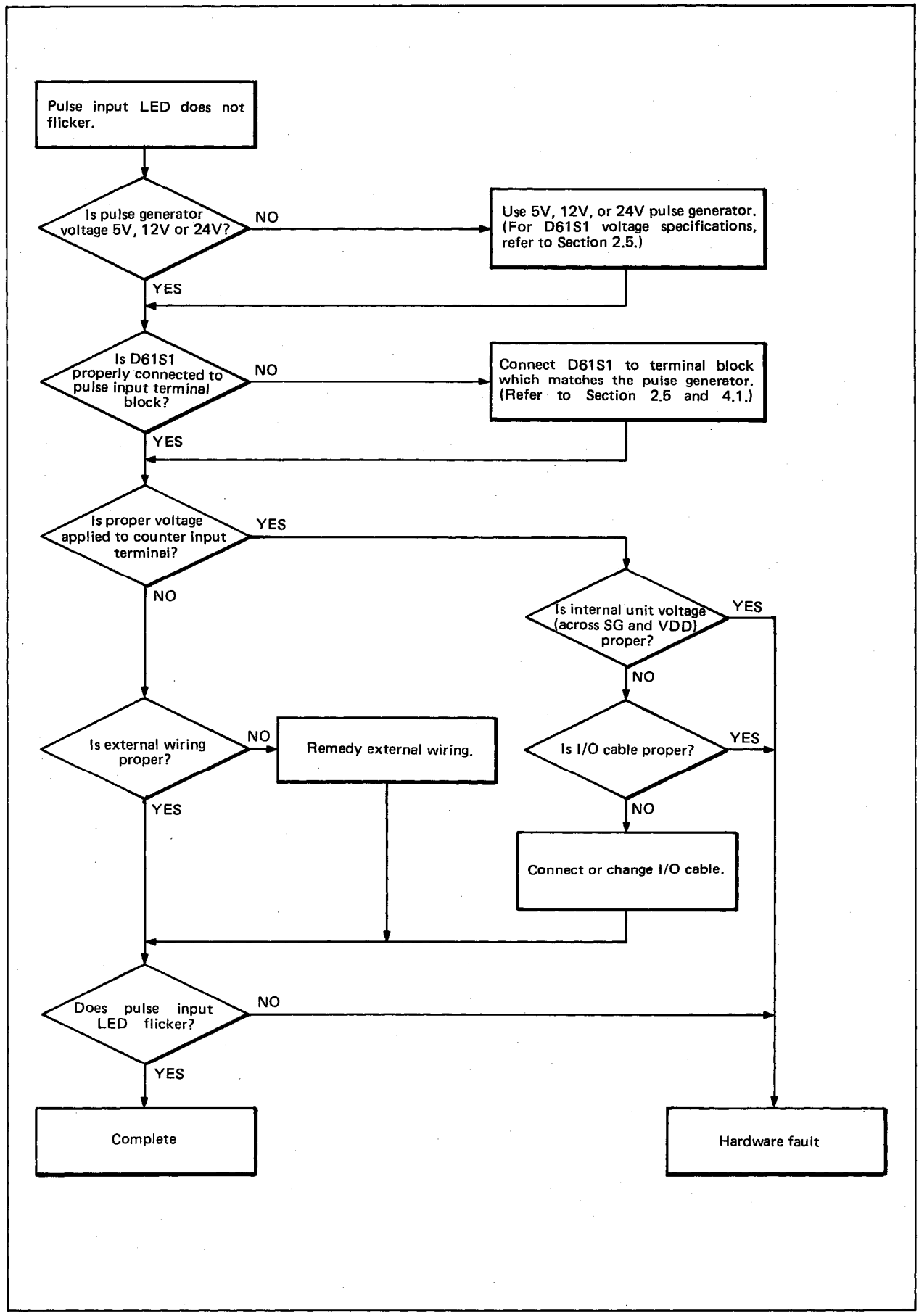
8. TROUBLESHOOTING

This chapter explains troubleshooting procedures for the D61S1. For the CPU unit, refer to the A0J2 Programming Manual.

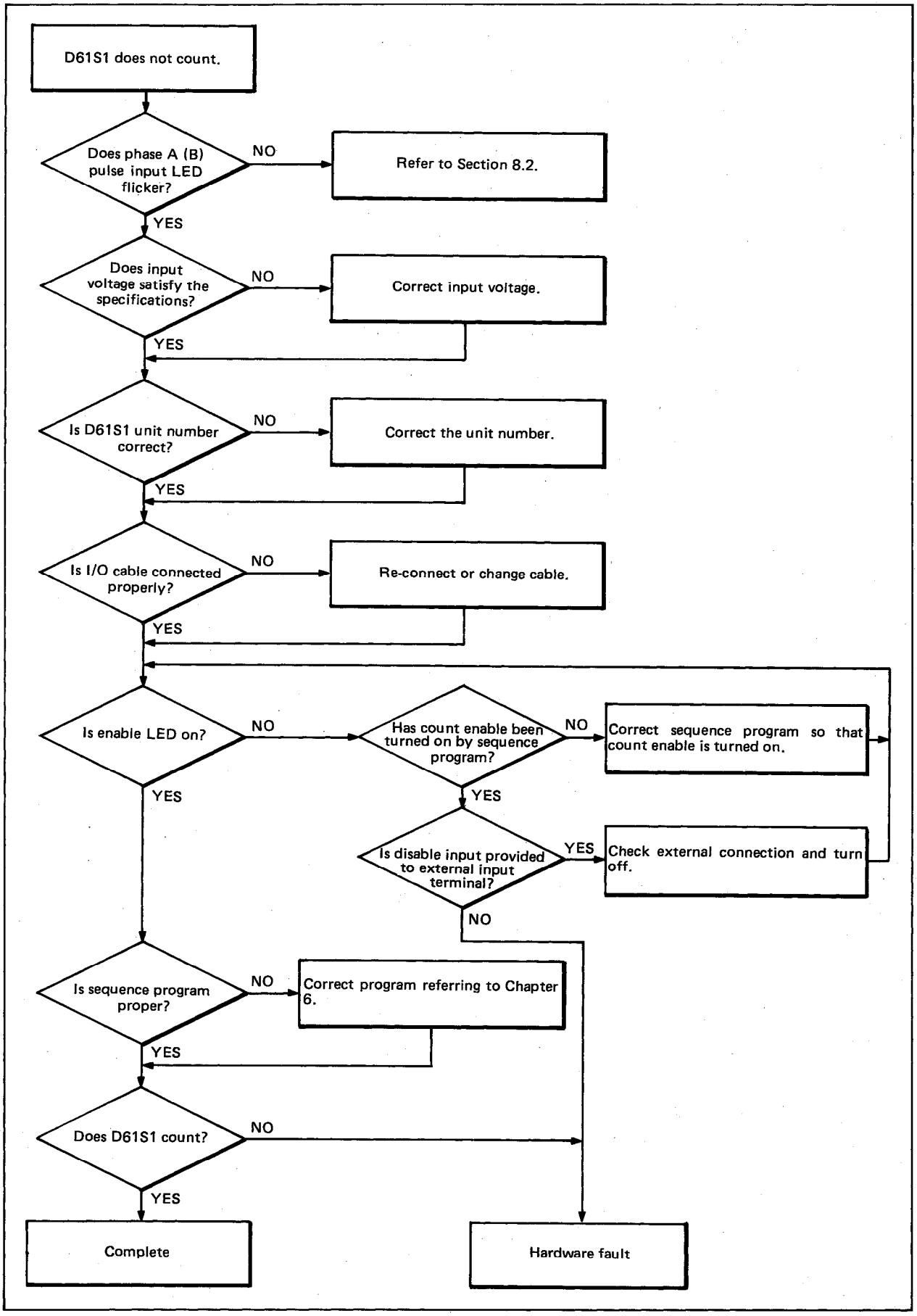
8.1 General Troubleshooting Flow Chart



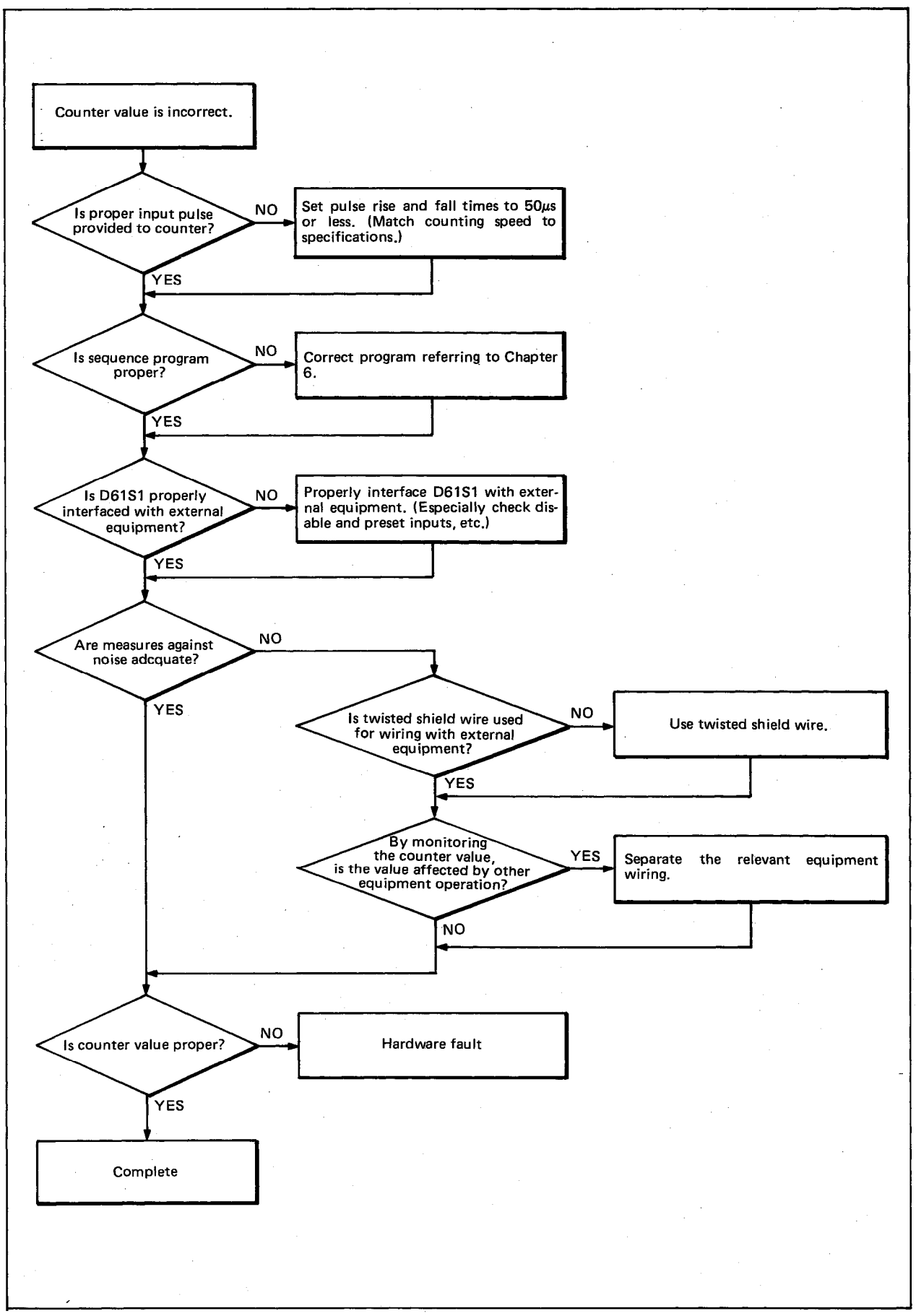
8.2 Flow Chart Used When Phase A(B) Pulse Input LED Does Not Flicker



8.3 Flow Chart Used When D61S1 Does Not Count



8.4 Flow Chart When Count Value Is Incorrect

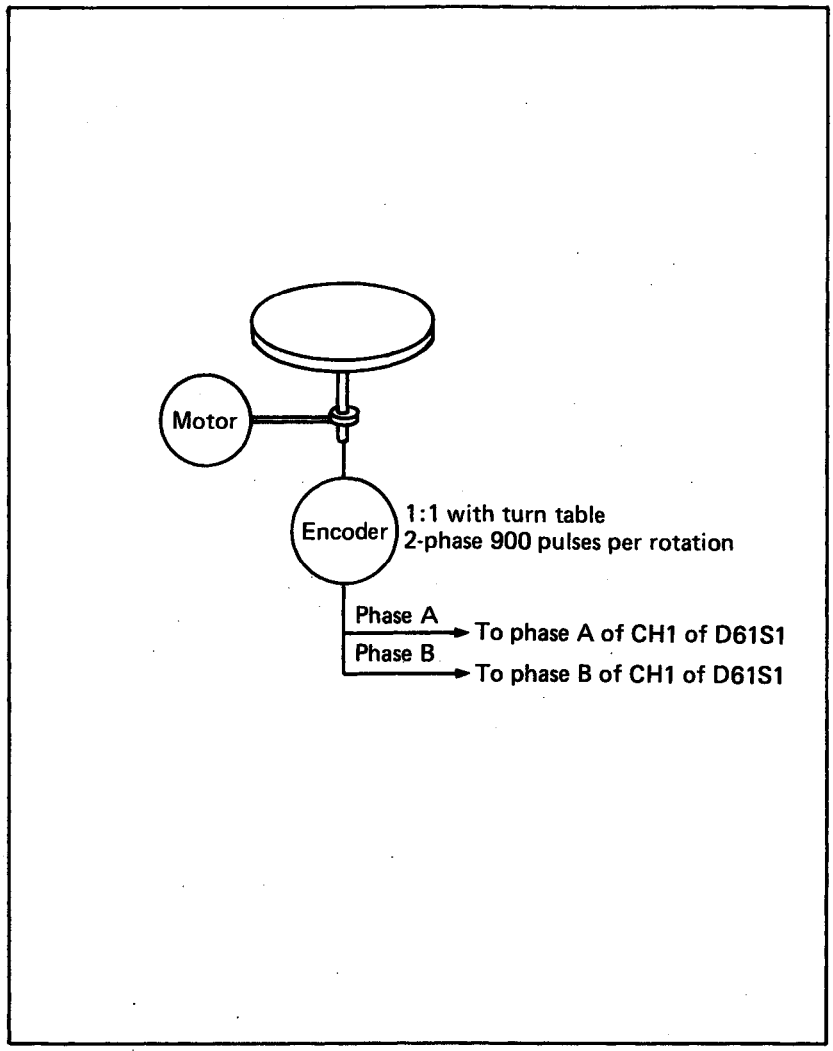


APPENDICES

APPENDIX 1 Application Circuit Examples

- Example of turn table indexing
- Example using ring counter function
- Example using CH1 and CH2 coincidence signal output

(1) Example of turn table indexing



Operation

The indexing table is positioned at a corresponding to the digital switch setting (0 to 3599). The encoder is directly connected to the turn table rotating shaft. The encoder gives 900 pulses per rotation, 2-phase.

I/O assignment

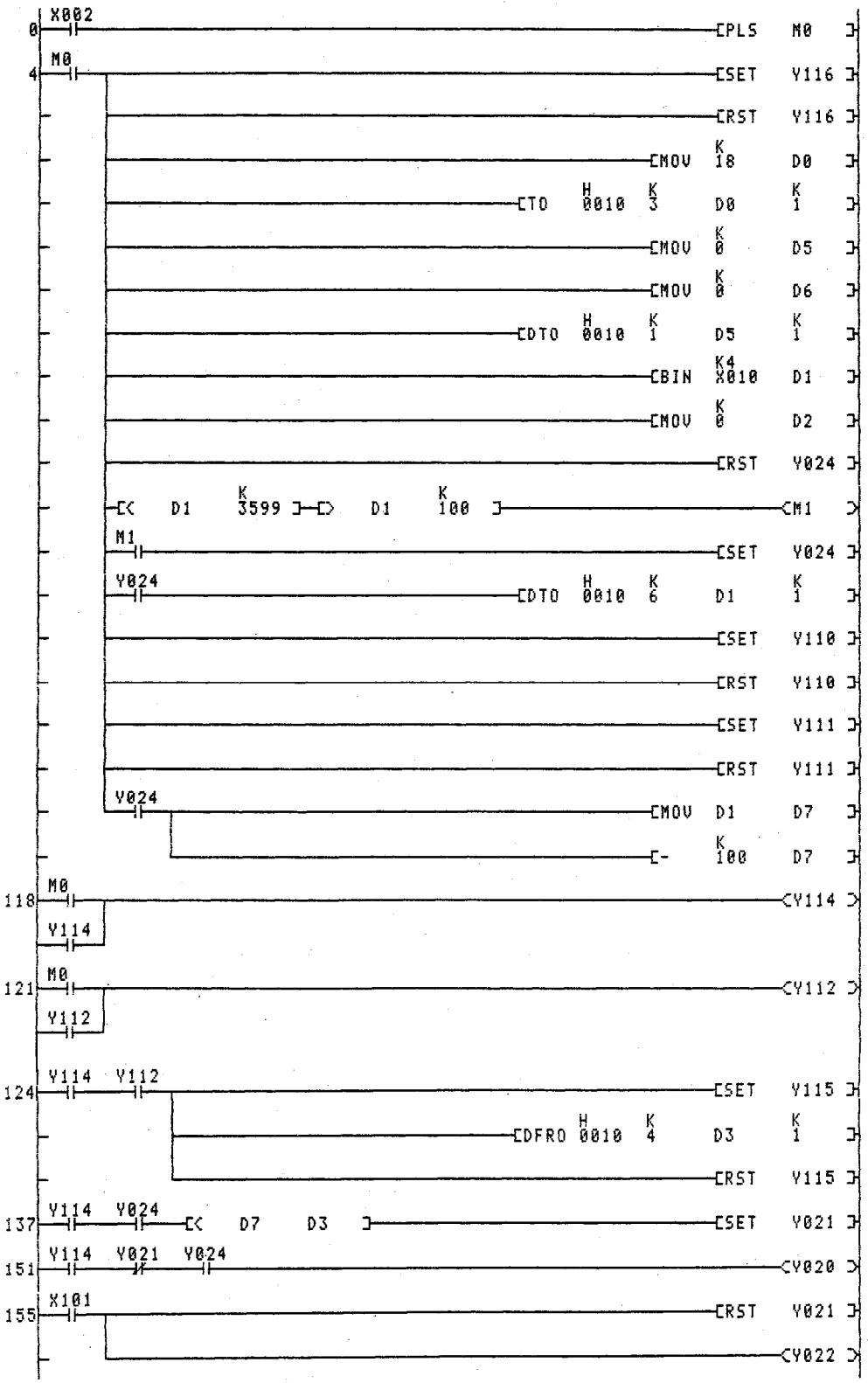
X/Y100 to X/Y11F	D61S1
X10 to X1F	4 digits of digital switch
X02	Start switch
Y20	Motor high speed
Y21	Motor low speed
Y22	Completion signal
Y24	Set value range OK

Data register assignment

D0	Mode
D1, D2	Set value
D3, D4	Present value
D5, D6	Preset value
D7	Deceleration point value

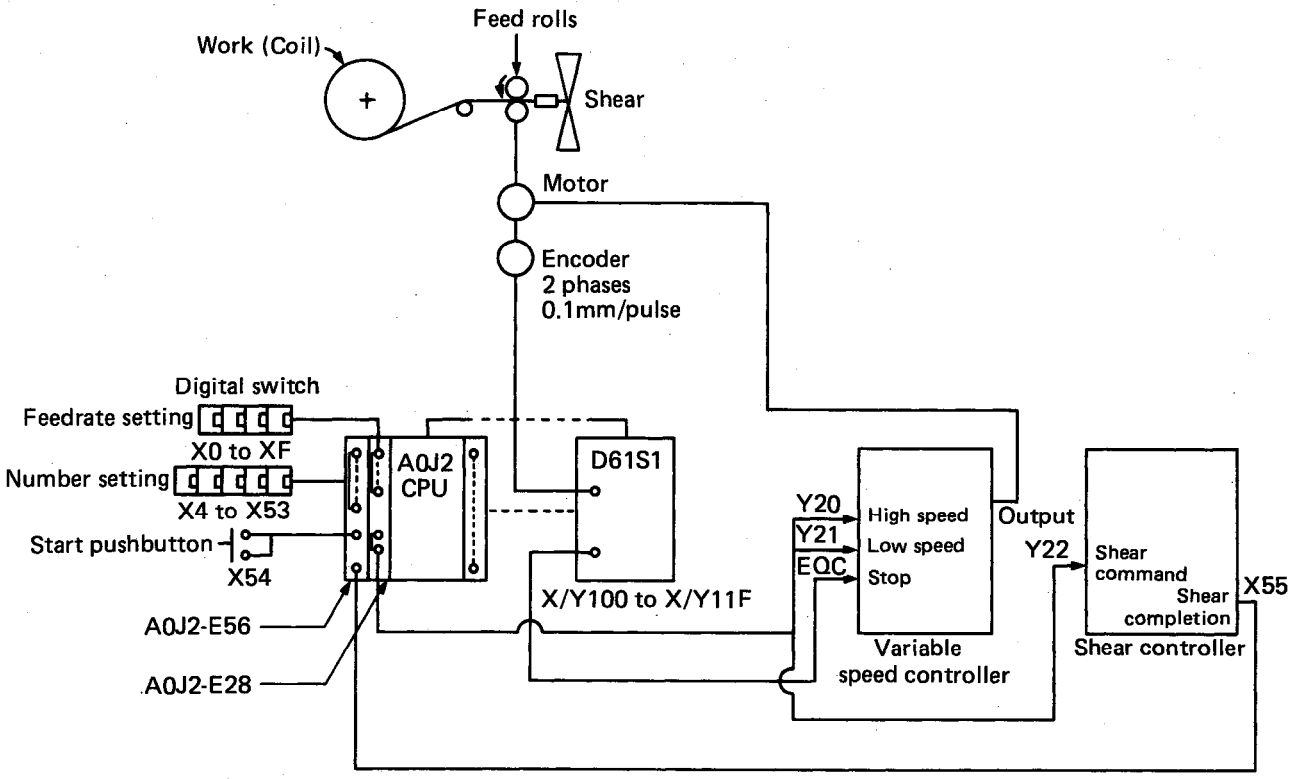
When the start pushbutton is pressed, the motor rotates at high speed and present the value is read. 10 degrees ahead of the indexing point, the speed is reduced. When the counter value coincidence signal turns on, the turn table is brought to a stop. (If the set value is 10 degrees (100 counts) or less, the program does not operate.)

Example of turn table indexing



(2) Example using ring counter function

Shearing control application using the ring counter function. (Set the ring counter setting switch to ON.)



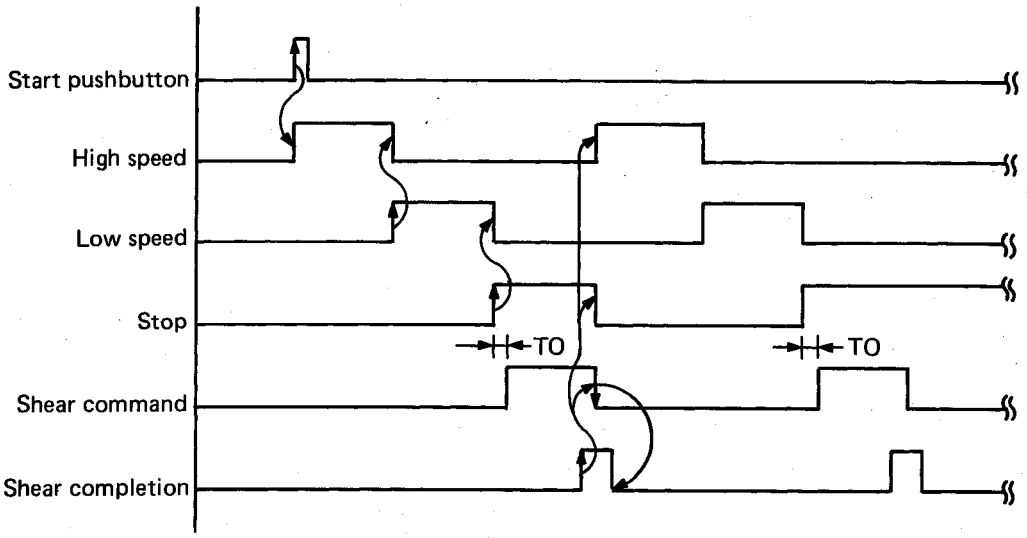
Operation

When the start pushbutton is pressed, the amount set by the feedrate digital switch is advanced. When positioning is completed, a shear command is sent to the shear controller. When shearing is complete, the positioning operation is repeated. (Deceleration point is 100 counts ahead of the set value. If the set value is 100 counts or less, the program does not operate.)
In this case, assume that the D61S1 is assigned to X/Y100 to X/Y11F.

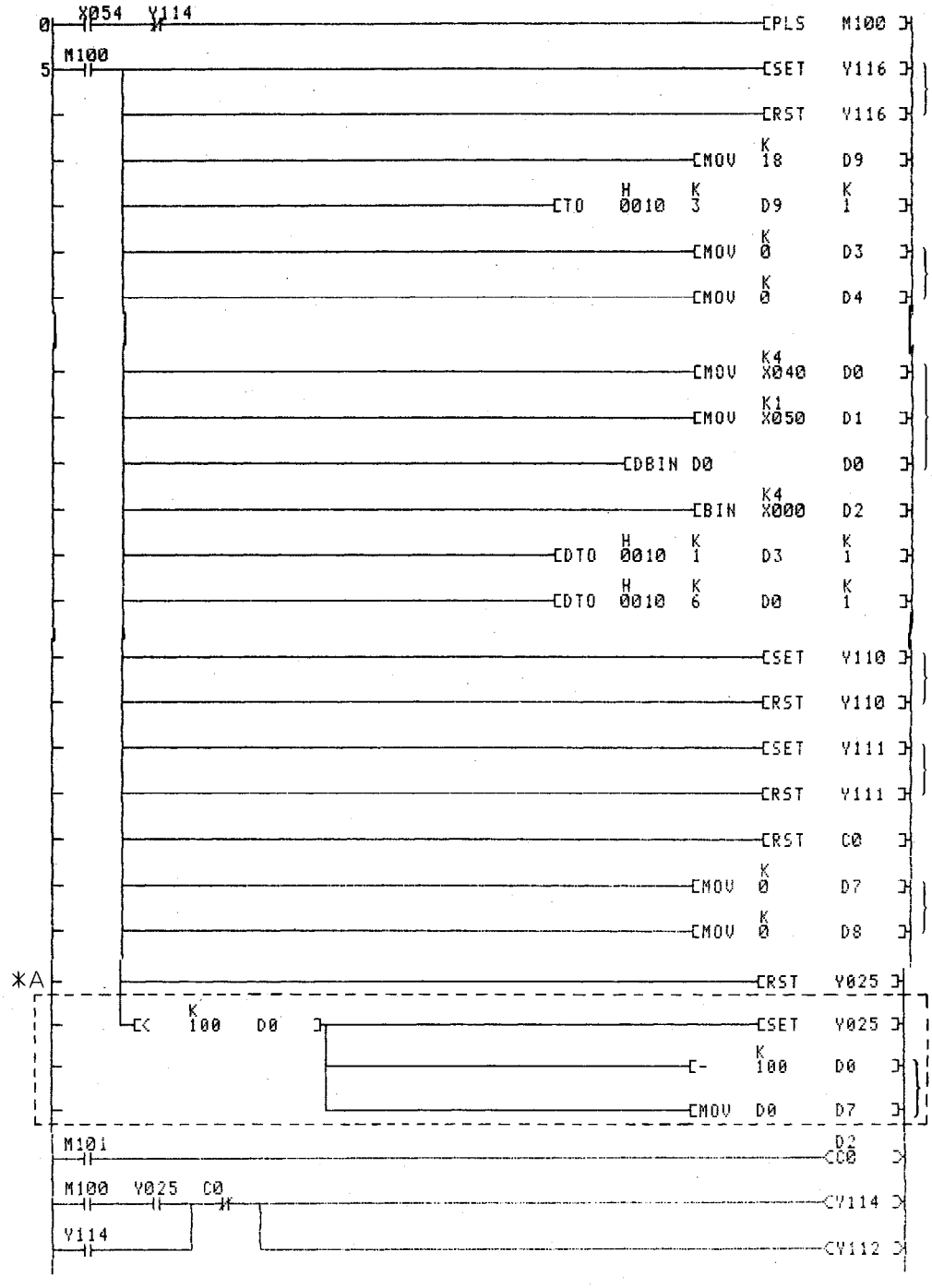
Data register assignment

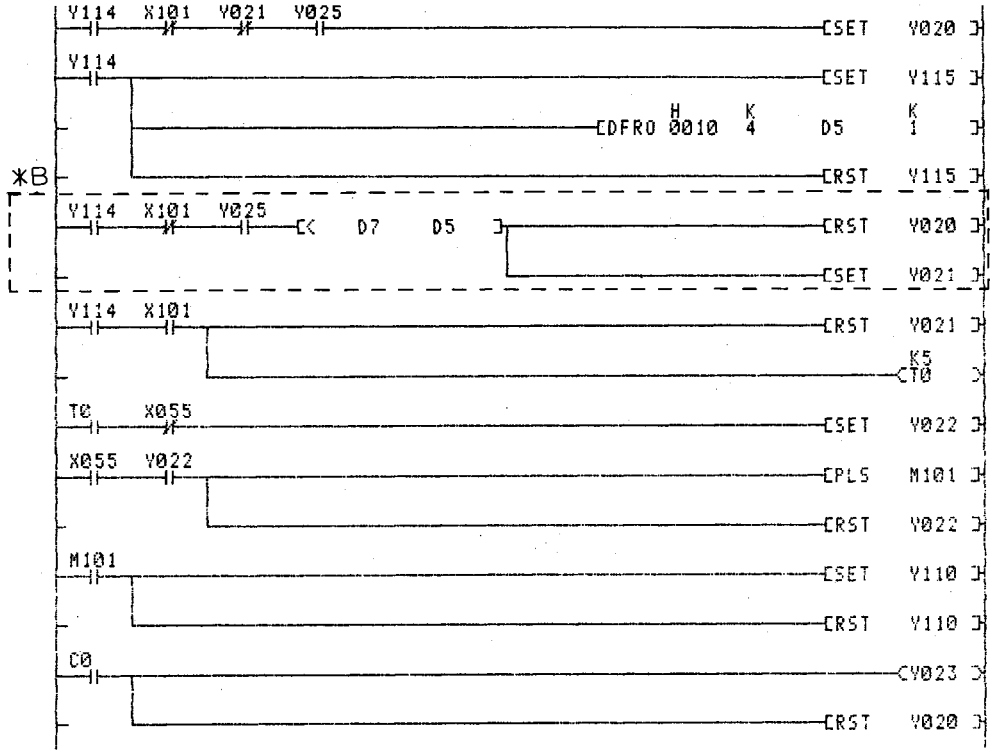
D0, D1	Set value
D2	Number value
D3, D4	Preset value
D5, D6	Present value
D7, D8	Deceleration point
D9	Mode

Operation timing
(Number setting = 2)



(A) Programming example when set value is 32767 or less





High speed command ON

Present value read request

Present value is read from buffer memory to data registers (D5, D6).

Low speed command ON

Dwell time

Shear command

Shear complete command

Coincidence signal reset

Completion signal

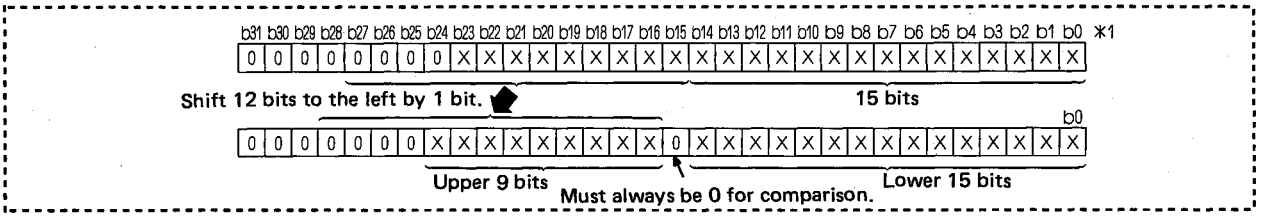
*A and *B indicate areas which are to be changed if the set value is 32768 to 16777215.

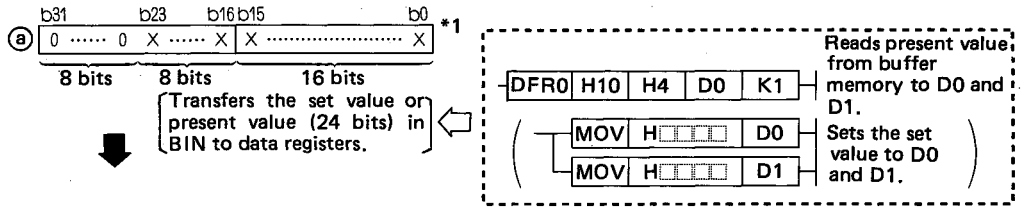
IB (NA) 66094-B

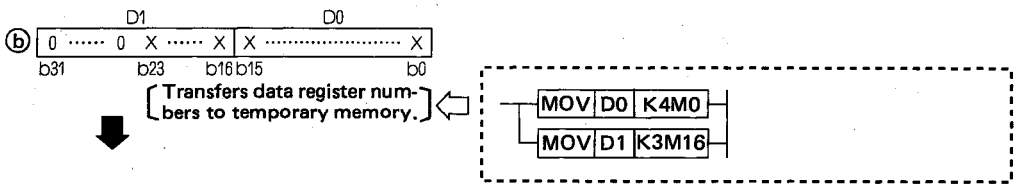
(B) Programming example when set value is in the range 32768 to 16777215
(The set value must be specified in D0 and D1 using MOV instruction.)

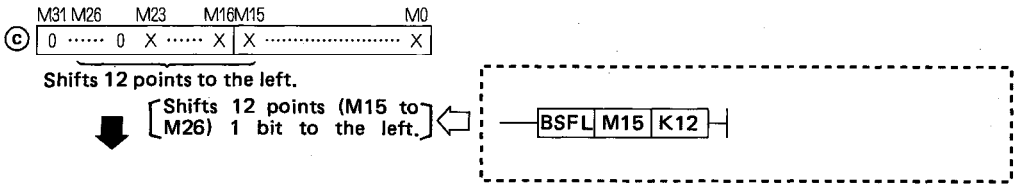
The D61S1 is capable of counting 24-bit BIN values (0 to 16777215). If this count value is used for operation with the A0J2CPU, only 16-bit BIN values (−32768 to +32767) are compared using a comparison instruction. Hence, it is necessary to use an idea in order to compare values of +32768 and more. Magnitude comparison procedures for +32768 and greater values are explained below.

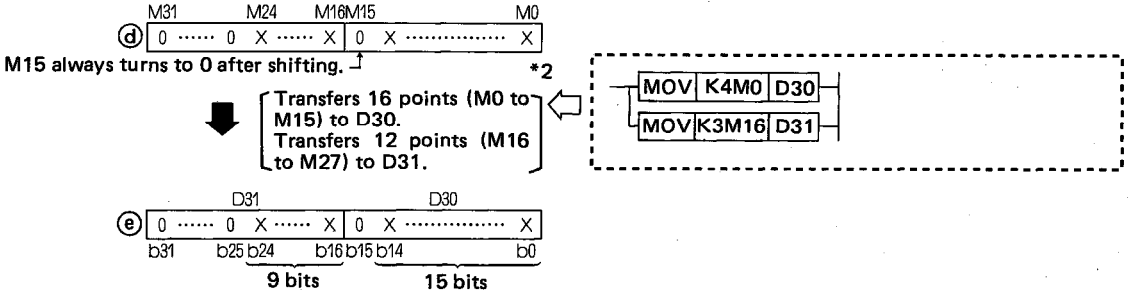
1) To compare 24-bit BIN values, divide 24 bits into lower 15 bits and upper 9 bits.
In 16-bit comparison, b0 to b14 represent a numeric value and b15 represents a positive or negative sign. Prior to comparison, always shift the bits as shown below and set 0 to b15.











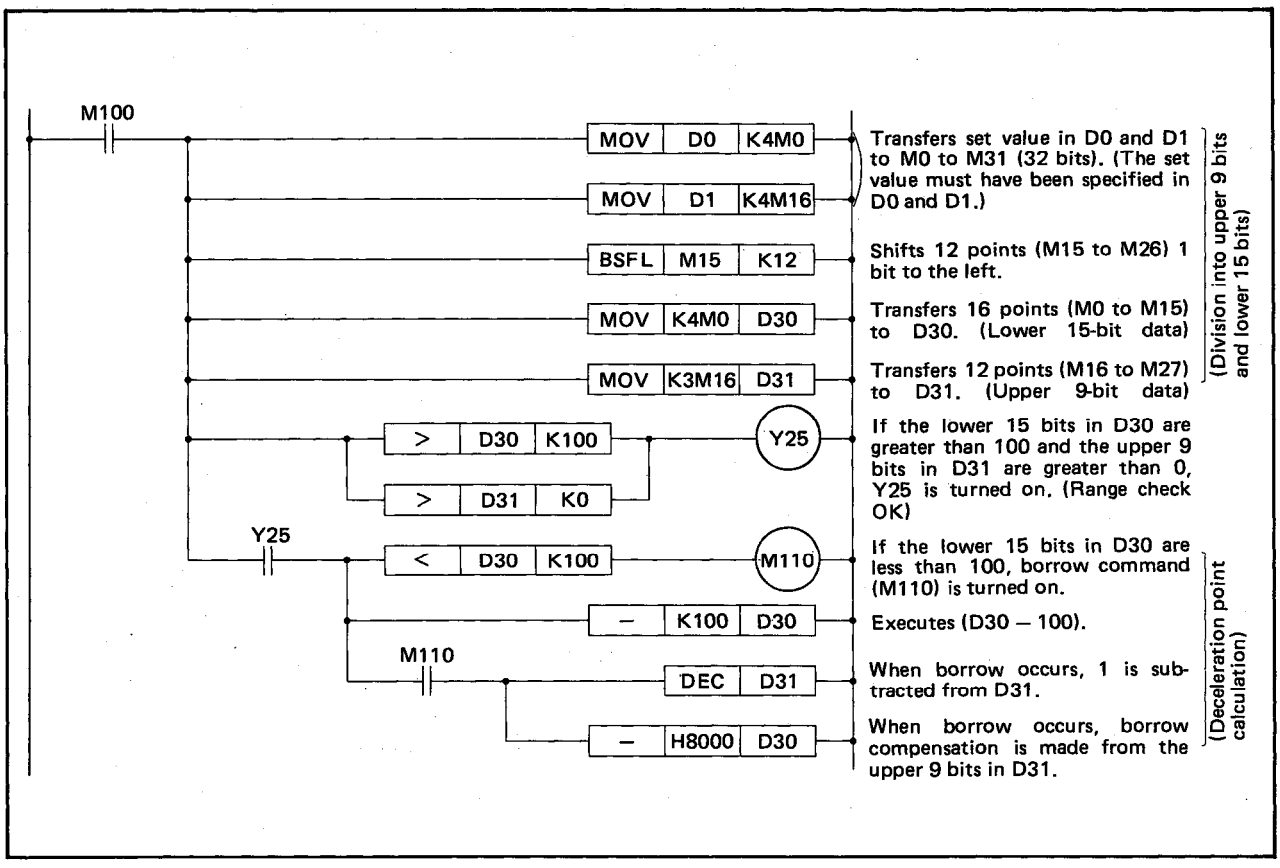
*1: ○ b0 to b31 represent the bits of 32-bit BIN data.
○ X in each bit indicates that the set value or present value is 0 or 1.

*2: In the 16-bit BIN comparison instruction, the sign depends on b15 setting; i.e. when 0 is in b15, the sign is positive and when 1, negative. Therefore, it is always necessary to shift b15 to b23 leftward and set 0 to b15 (M15).

2) To compare data divided into upper 9 and lower 15 bits

a) Make magnitude comparison of the upper 9 bits.
b) If the upper 9 bits are the same, compare the lower 15 bits.

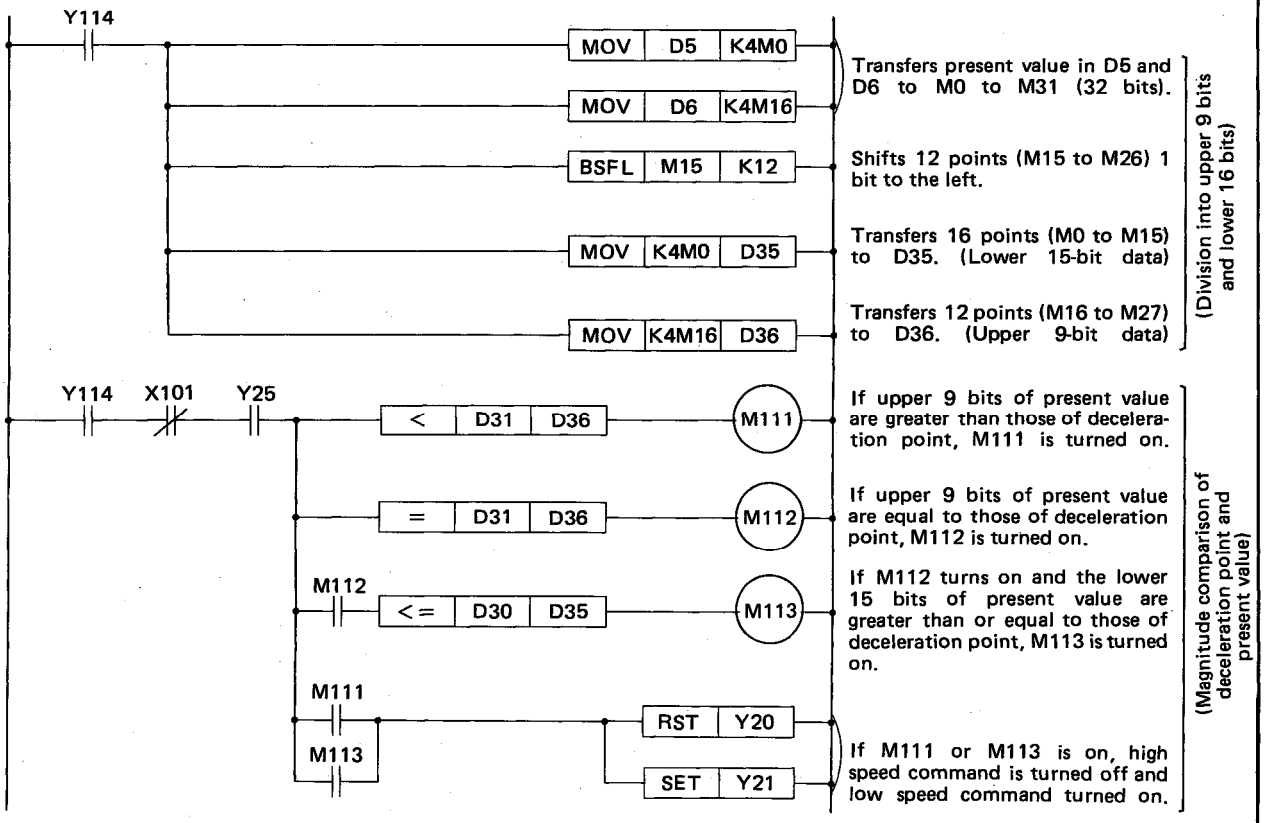
*Program example for area A (page APP-5)



*Program example for area B (page APP-6)

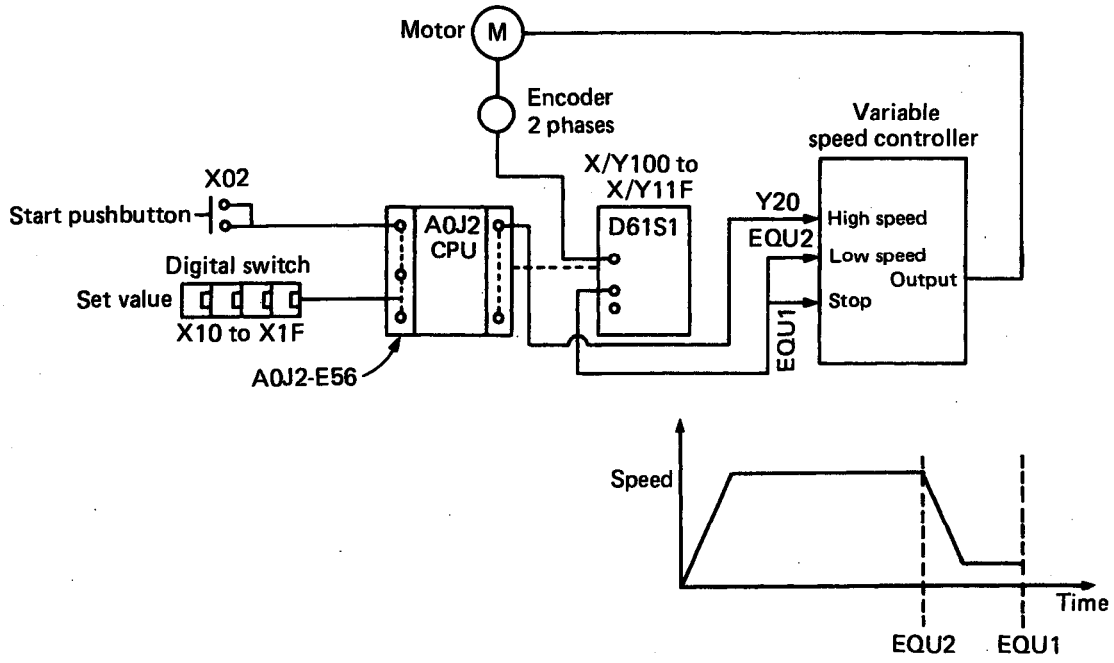
Change the data registers in 1) as shown below.

D0, D0 to D5, D6
D30, D31 to D35, D36



(3) Example using CH1 and CH2 coincidence signal output

This section shows a high-speed response positioning circuit example which uses the coincidence signal outputs of CH1 and CH2 (EQU1 and EQU2) and has no relation to the scan time of the sequence program.
(Connect the pulse outputs of the encoder to CH1 and CH2 of the D61S1. Also, specify set values in 4-digit BCD.)

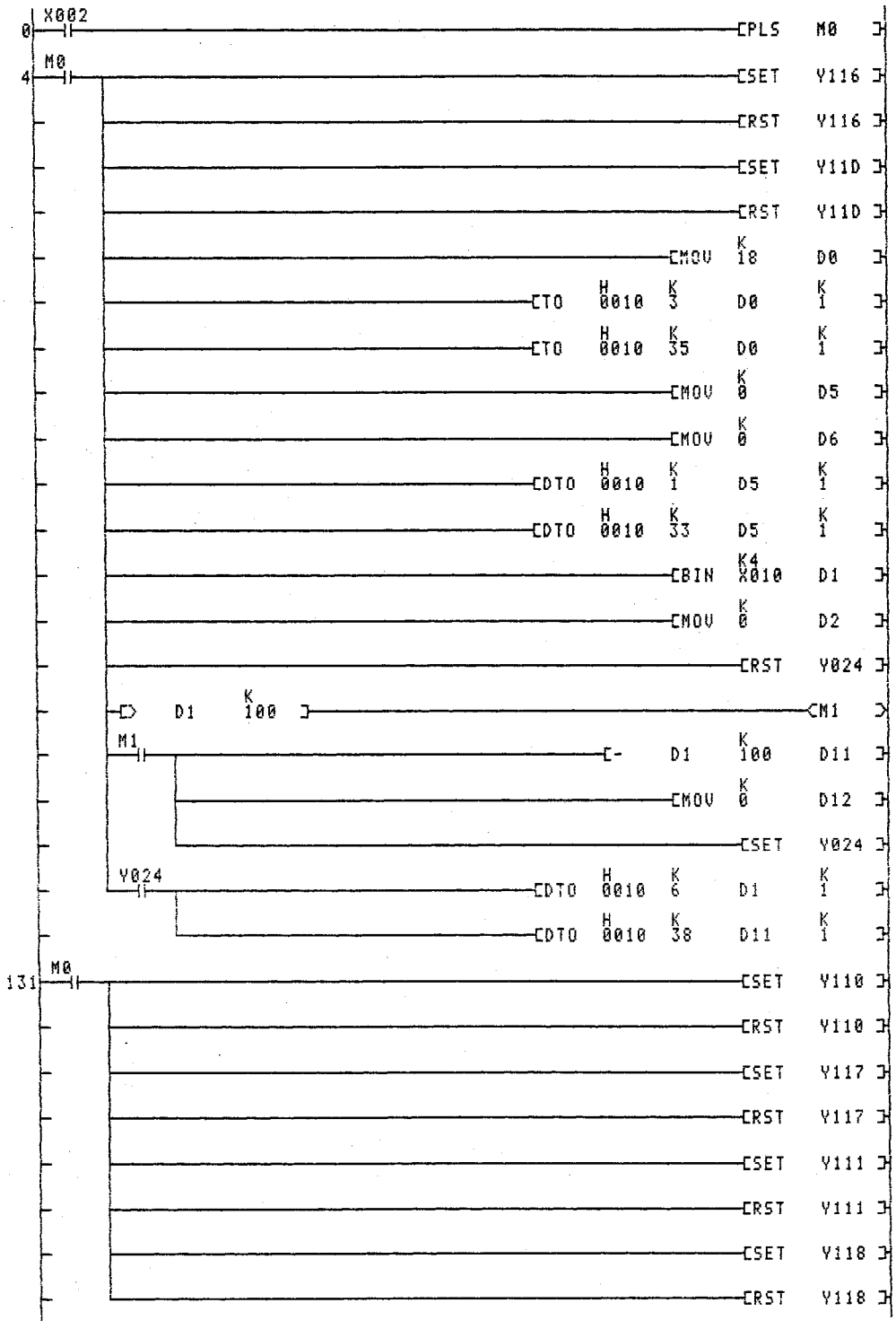


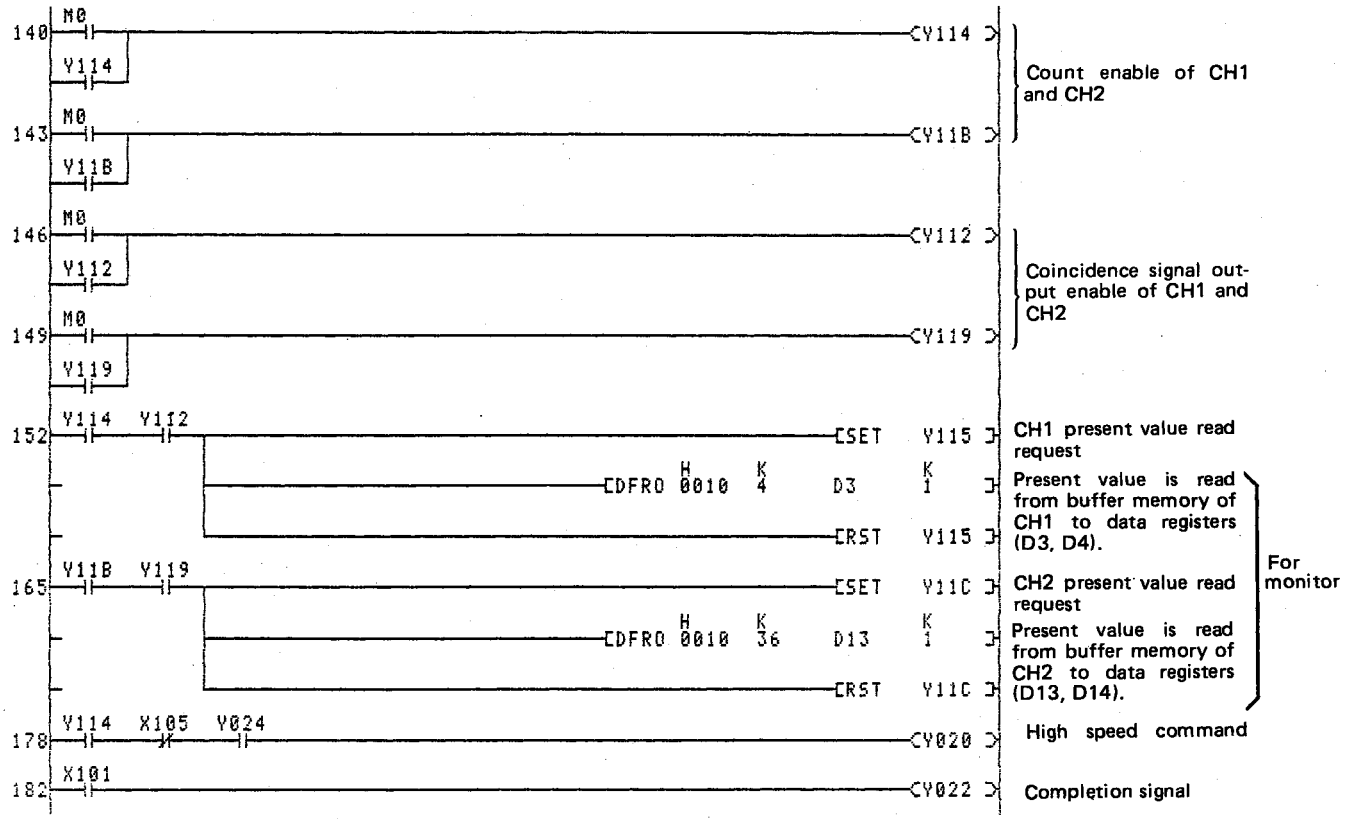
Operation

When the start pushbutton is pressed, the set value is read from the digital switch, output Y is provided, and positions the job at high-speed, using the output signals EQU1 and EQU2.
(Deceleration point is 100 counts ahead of set value. If the set value is 100 counts or less, program does not operate.)
In this case, assume that the D61S1 is assigned to X/Y100 to X/Y11F.

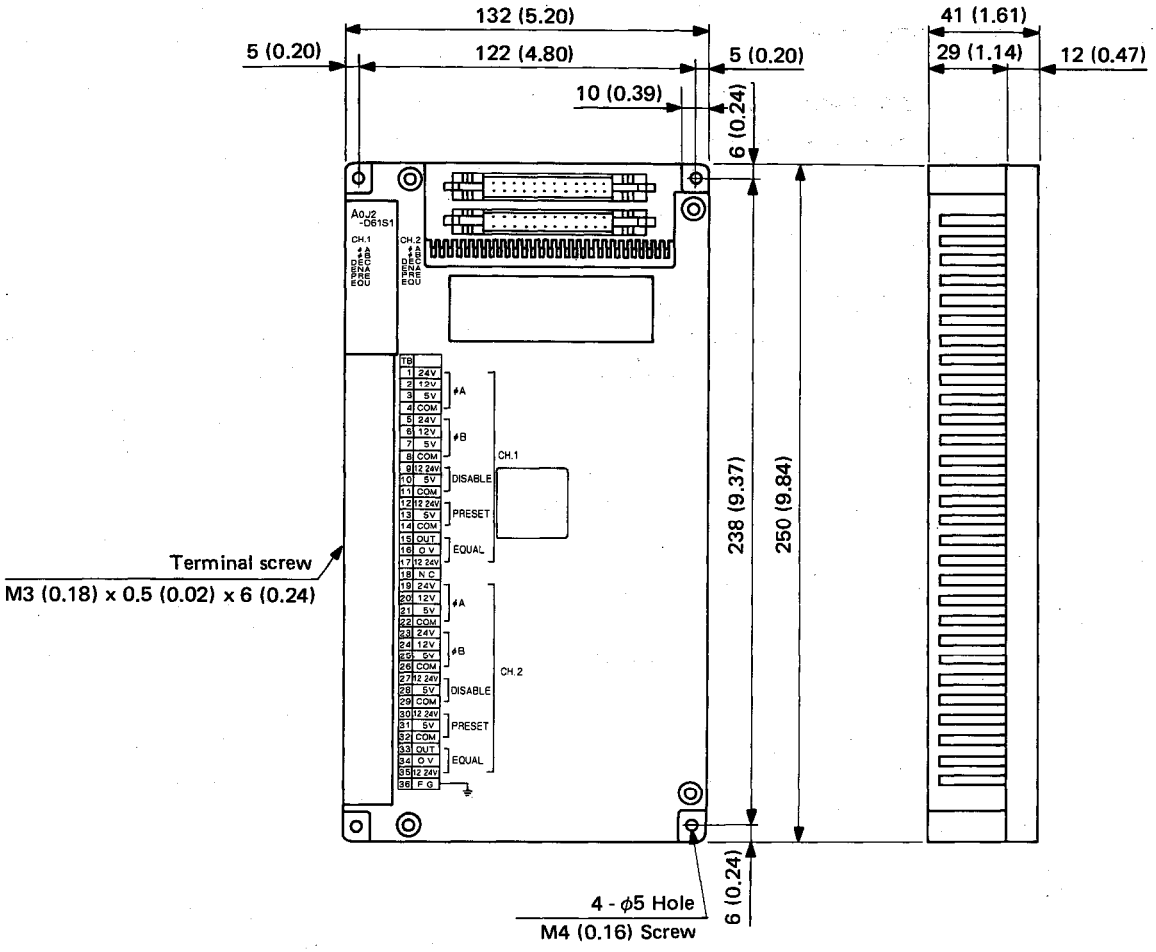
Data register assignment

D0	Modes of CH1 and CH2
D1, D2	Set value of CH1
D3, D4	Present value of CH1
D5, D6	Preset values of CH1 and CH2
D11, D12	Set value of CH2
D13, D14	Present value of CH2


X002
PLS M0
Start pulse
M0
SET Y116
RST Y116
SET Y11D
RST Y11D
CH1 and CH2 external preset detection reset
MOV K18 D0
Constant of 2 phases is written to data register.
TO H0010 K3 D0 K1
TO H0010 K35 D0 K1
Mode is written to buffer memories of CH1 and CH2.
MOV K0 D5
MOV K0 D6
Preset value is written to data registers (D5, D6).
DTO H0010 K1 D5 K1
DTO H0010 K33 D5 K1
Preset value is written to buffer memories of CH1 and CH2 (D5, D6).
BIN K4X010 D1
MOV K0 D2
RST Y024
Set value is read from digital switch to data registers (D1, D2). (For set value, specify 4 times of required pulse input.)
D1 K100
M1
Set value range check OK
- D1 K100 D11
MOV K0 D12
Calculation of deceleration point (D11, D12)
SET Y024
Y024
DTO H0010 K6 D1 K1
Set value (stop point) is written to buffer memory of CH1.
DTO H0010 K38 D11 K1
Set value (deceleration point) is written to buffer memory of CH2.
M0
SET Y110
RST Y110
SET Y117
RST Y117
Coincidence signals of CH1 and CH2 are reset.
SET Y111
RST Y111
SET Y118
RST Y118
Preset commands of CH1 and CH2


140 M0
Y114
Y114
143 M0
Y11B
Y11B
Count enable of CH1 and CH2
146 M0
Y112
Y112
149 M0
Y119
Y119
Coincidence signal output enable of CH1 and CH2
152 Y114 Y112
SET Y115
CH1 present value read request
DFRO H0010 K4 D3 K1
Present value is read from buffer memory of CH1 to data registers (D3, D4).
RST Y115
165 Y11B Y119
SET Y11C
CH2 present value read request
DFRO H0010 K36 D13 K1
Present value is read from buffer memory of CH2 to data registers (D13, D14).
RST Y11C
For monitor
178 Y114 X105 Y024
Y020
High speed command
182 X101
Y022
Completion signal

APPENDIX 2 External View



Unit : mm (inch)

WARRANTY

Please confirm the following product warranty details before starting use.

1. Gratis Warranty Term and Gratis Warranty Range

If any faults or defects (hereinafter "Failure") found to be the responsibility of Mitsubishi occurs during use of the product within the gratis warranty term, the product shall be repaired at no cost via the dealer or Mitsubishi Service Company. Note that if repairs are required at a site overseas, on a detached island or remote place, expenses to dispatch an engineer shall be charged for.

[Gratis Warranty Term]

The gratis warranty term of the product shall be for one year after the date of purchase or delivery to a designated place.

Note that after manufacture and shipment from Mitsubishi, the maximum distribution period shall be six (6) months, and the longest gratis warranty term after manufacturing shall be eighteen (18) months. The gratis warranty term of repair parts shall not exceed the gratis warranty term before repairs.

[Gratis Warranty Range]

(1) The range shall be limited to normal use within the usage state, usage methods and usage environment, etc., which follow the conditions and precautions, etc., given in the instruction manual, user's manual and caution labels on the product.

(2) Even within the gratis warranty term, repairs shall be charged for in the following cases.

1. Failure occurring from inappropriate storage or handling, carelessness or negligence by the user. Failure caused by the user's hardware or software design.
2. Failure caused by unapproved modifications, etc., to the product by the user.
3. When the Mitsubishi product is assembled into a user's device, Failure that could have been avoided if functions or structures, judged as necessary in the legal safety measures the user's device is subject to or as necessary by industry standards, had been provided.
4. Failure that could have been avoided if consumable parts (battery, backlight, fuse, etc.) designated in the instruction manual had been correctly serviced or replaced.
5. Failure caused by external irresistible forces such as fires or abnormal voltages, and Failure caused by force majeure such as earthquakes, lightning, wind and water damage.
6. Failure caused by reasons unpredictable by scientific technology standards at time of shipment from Mitsubishi.
7. Any other failure found not to be the responsibility of Mitsubishi or the user.

2. Onerous repair term after discontinuation of production

(1) Mitsubishi shall accept onerous product repairs for seven (7) years after production of the product is discontinued. Discontinuation of production shall be notified with Mitsubishi Technical Bulletins, etc.

(2) Product supply (including repair parts) is not possible after production is discontinued.

3. Overseas service

Overseas, repairs shall be accepted by Mitsubishi's local overseas FA Center. Note that the repair conditions at each FA Center may differ.

4. Exclusion of chance loss and secondary loss from warranty liability

Regardless of the gratis warranty term, Mitsubishi shall not be liable for compensation to damages caused by any cause found not to be the responsibility of Mitsubishi, chance losses, lost profits incurred to the user by Failures of Mitsubishi products, damages and secondary damages caused from special reasons regardless of Mitsubishi's expectations, compensation for accidents, and compensation for damages to products other than Mitsubishi products and other duties.

5. Changes in product specifications

The specifications given in the catalogs, manuals or technical documents are subject to change without prior notice.

6. Product application

(1) In using the Mitsubishi MELSEC programmable logic controller, the usage conditions shall be that the application will not lead to a major accident even if any problem or fault should occur in the programmable logic controller device, and that backup and fail-safe functions are systematically provided outside of the device for any problem or fault.

(2) The Mitsubishi general-purpose programmable logic controller has been designed and manufactured for applications in general industries, etc. Thus, applications in which the public could be affected such as in nuclear power plants and other power plants operated by respective power companies, and applications in which a special quality assurance system is required, such as for Railway companies or National Defense purposes shall be excluded from the programmable logic controller applications.

Note that even with these applications, if the user approves that the application is to be limited and a special quality is not required, application shall be possible.

When considering use in aircraft, medical applications, railways, incineration and fuel devices, manned transport devices, equipment for recreation and amusement, and safety devices, in which human life or assets could be greatly affected and for which a particularly high reliability is required in terms of safety and control system, please consult with Mitsubishi and discuss the required specifications.

High Speed Counter Module for A0J2 Type A0J2-D61S1

User's Manual

MODEL	A0J2-D61S1-USE-E
MODEL CODE	13J613
IB(NA)-66094-C(0312)MEE	

MITSUBISHI ELECTRIC CORPORATION

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Specifications subject to change without notice.